Design of Integrated Readout Circuit for NMOS THz Detectors Based on Chopper Amplifier Concept

Cezary Kołaciński, Dariusz Obrębski, and Przemysław Zagrajek

***Abstract*—This paper deals with design of readout circuit dedicated for NMOS-based terahertz detectors. The proposed architecture bases on chopper amplifier and instrumentation amplifier concepts. The main objectives were high gain (max. 100 dB) and proper operation with NMOS-based THz detectors. Three different architectures of measurement amplifier designed for the research project are discussed in this paper. The designed chip was manufactured in AMS C35B4 process (350 nm feature size). Another issue described in this paper is dedicated, non-typical testing environment. At the end a few measurement results are shown.**

***Index Terms*—NMOS-based Terahertz detector, chopper amplifier, instrumentation amplifier, voltage controlled amplifier, programmable gain amplifier, readout circuit**

I. Introduction

PLASMONIC field-effect transistors (FETs) have gained much attention for THz detection [1],[2],[3]. The use of FET as THz detector was first proposed by Dyakonov and Shur in [4]. The theory bases on analogy between equations of the electron transport in a gated two-dimensional transistor channel and those of shallow water or acoustic waves in music instruments. A THz signal applied between the source and the gate electrodes, self-rectifies by interaction of the two-dimensional electron gas (2DEG) in the transistor channel [5], the drain is typically treated as output of the detector. Electron ballistic transport enables then the FET response at the frequencies considerably higher than the device cut-off frequency.

Design of readout circuit, matching the response of THz-irradiated FET, is a complicated task. The signal originated from the detector output is a very low DC voltage (i.e. several μV) [6], [7] and [8]. Thus the prerequisites for such kind of circuit are high gain and low noise. Another important properties are: high input impedance and the gain controlled in a wide range - needed to match the detector electrical parameters, as well as its response [9]. The proposed architecture of the readout circuit is based on the chopper amplifier concept what guarantees achieving the mentioned expectations. Three different variants of that circuit are presented in this paper, and the electrical design at transistor level, as well as layout issues are discussed in details.

C. Kołaciński, D. Obrębski are with ICs and Systems Design Department, Institute of Electron Technology, Warsaw, Poland. (ckolacin@ite.waw.pl, obrebski@ite.waw.pl)

P. Zagrajek is with Institute of Optoelectronics, Military University of Technology, Poland (pzagrajek@wat.edu.pl).

The next important task, covered by this paper is related to non-typical measurements of prototype ICs. Two different measurement boards have been developed, the first one was used for characterization of the samples, while the second one was intended for tests in target application, i.e. with THz detector at the input and THz source. It is worth to notice, that each prototype contains three different variants of the readout circuits, plus one equipped with on-chip detector, what made the number of input and output signals in measurement setup considerable. Another important issue related to prototypes characterization was development of the adjustable, low noise, low amplitude DC source needed as replacement for an NMOS-based THz detector. For that task special circuit with two J-type thermocouples has been used. This paper describes also problems encountered during very low signals measurement and some solutions applied to overcome them. The last part contains measurements results (for both applications boards) and a discussion about them. Finally some further improvements of readout circuit are proposed.

II. Chopper Amplifier

As it was written in the previous section, chopper amplifier architecture was chosen as one providing high gain and low noise benefits. Principle of operation of this kind of circuit is based on observation that it is quite easier to design a good AC voltage amplifier rather than a DC voltage one. The idea is straightforward: first a DC signal is modulated (e.g. by CMOS switching), next it is amplified by an AC gain stage, and - at the end - it is demodulated to a DC signal again. Diagram that explains this mechanism is shown in Figure 1.

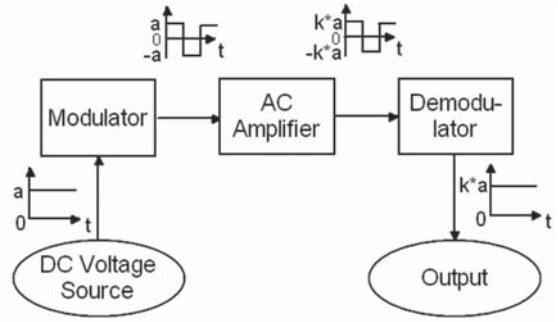

Fig. 1. The idea of chopper amplifier

The signal from DC voltage source is the input signal for circuit called modulator. Its task is to convert the DC voltage

a into the AC signal of *a* amplitude. Next this signal is amplified by an AC gain stage what produces output signal of *k*a* amplitude. Finally, block called demodulator converts this square wave again into DC signal of value *k*a*. That circuit concept has two fundamental benefits. First, it cancels the input offset voltage, because only AC component is amplified. This is the dynamic offset cancellation technique - it takes place when the amplifier is working. The second big advantage is *1/f* noise reduction. As the name suggests, it is a kind of noise with spectral power density increasing with decreasing frequency. For amplification of small DC voltage signals just this type of noise dominates over the second potential source of noise in MOSFET transistors - the thermal noise. Both features mentioned above are strongly recommended for discussed readout circuit and are the main causes of choosing the chopper amplifier architecture.

A. Modulator

The modulator converts DC voltage signal of *a* value into a square wave of *a* amplitude. This is a simple task and it could be realized by the basic circuit using four CMOS switches (transmission gates). This architecture is shown in Figure 2.

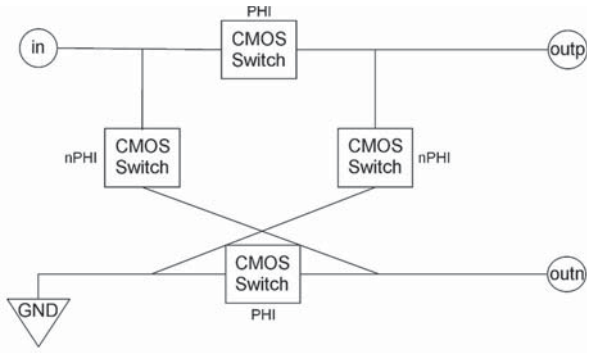

Fig. 2. Modulator architecture

There are two pairs of switches - first of them is controlled by signal *PHI* and second one by signal *nPHI* (PHI negation). This circuit has two modes of operation: in the first one the top/bottom switches are on and the left/right are off - *in* signal appears at output *outp*, *outn* is grounded. In the second mode the situation is strictly opposite: top/bottom switches are off, left/right are on and *in* signal appears at *outn*. The switching frequency in this case is not a critical parameter, because the detector response is not expected to change too fast. On the other hand, it determines the f_{chop} frequency for whole chopper amplifier. Arbitrarily $f_{chop} = 1\ kHz$ has been chosen, so the input signal can not change faster than 500 times per second ($f = 500\ Hz$ is the Nyquist frequency).

B. AC Amplifier

The AC amplifier amplifies square wave signal coming from the modulator. Main requirements for this circuit are: high input impedance, high gain and immunity to interferences. These features can be achieved in architecture called instrumentation amplifier. The schematic of the AC amplifier, which bases on instrumentation amplifier topology, is shown in Figure 3 (see next page).

In proposed circuit, in respect to the traditional instrumentation amplifier architecture, the input stage has been doubled. It was done, because in single-staged circuit it is relatively hard to achieve the high gain because of required $R_{f1/f2}$ to $R_{11/12}$ ratio (see Figure 3). According to (1) - to provide the high gain - $R_{f1/f2}$ value has to be very high or $R_{11/12}$ has to be very low. Both cases cause some drawbacks in IC implementation. High resistance can be achieved using high-resistive polysilicon layer, which is characterized by high relative variations of resistance. On the other hand, ability to use low resistances is limited by process design rules (i.e. minimum number of squares for polysilicon resistor). Using two input stages in series results in their gains to be multiplied (in linear scale) and makes it possible to apply moderate value of resistances in each stage.

It is important to notice that circuit presented in Figure 3 ensures also high input impedance and allows simple gain control by changing the R_{11} and R_{12}. Its output stage contains the operational amplifier in differential configuration. This property enables to achieve the high Common Mode Rejections Ratio (CMRR). It is very important because of noise contributed by CMOS switches in modulator.

The gain of the amplifier presented in Figure 3 is given by equation (1).

$$k_u = -\frac{R_3}{R_2}(1 + 2\frac{R_{f1}}{R_{11}})(1 + 2\frac{R_{f2}}{R_{12}}) \tag{1}$$

Analysis of the voltage signals leads to the three equations: (2), (3) and (4) (with symbols corresponding to Figure 3).

$$a_2(t) = \frac{1}{2} \cdot k_1 \cdot k_2 \cdot V_{in}(t) + \frac{1}{2}\sum_{j=1}^{n=2} k_j ... \cdot k_n \cdot (Vio1_j - Vio2_j) \tag{2}$$

$$a_2(t)' = -\frac{1}{2} \cdot k_1 \cdot k_2 \cdot V_{in}(t) - \frac{1}{2}\sum_{j=1}^{n=2} k_j ... \cdot k_n \cdot (Vio1_j - Vio2_j) \tag{3}$$

$$out_2(t) = a_2(t) - a_2(t)' = \underbrace{k_1 \cdot k_2 \cdot V_{in}(t)}_{desirable} + \underbrace{\sum_{j=1}^{n=2} k_j ... \cdot k_n \cdot (Vio1_j - Vio2_j)}_{undesirable} \tag{4}$$

Equation (4) shows that after the *n* gain stages (in our particular case - two) output signal contains two components: first one - desirable - which is an input voltage multiplied by gains; and the second one - undesirable - that contains the difference between the input offset voltages of operational amplifiers. To minimize that unwanted component the offset voltages of used operational amplifiers should be as equal

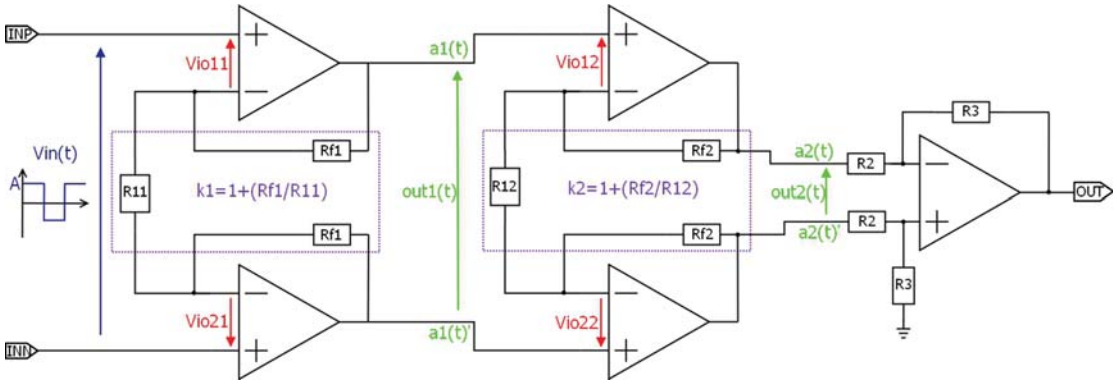

Fig. 3. Architecture of used instrumentation amplifier

as possible. To achieve that, special cell containing two operational amplifiers has been designed. These amplifiers are electrically independent, but their layouts have been combined, resulting in minimization of input offset voltage difference.

As the NMOS detector response is proportional to the intensity of THz radiation, the ability to adjust the gain of readout circuit towards the range of input signal from the detector is the next desired feature. There are two basic types of Variable Gain Amplifiers (VGA), each one has different method of gain control:

- Voltage Controlled Amplifier (VCA). This is a device that adjusts its gain in proportional manner in response to the applied control voltage signal. The control is pure analog, gain can be changed continuously within the chosen range.
- Programmable Gain Amplifier (PGA). This is an amplifier which gain can be controlled by external digital signals.

The concepts of VCA and PGA were utilized in some of three variants of designed readout circuit. This guarantees gain control in a very wide range.

C. Demodulator

The demodulator block converts square wave signal of *a* amplitude into a DC voltage signal of *a* value. There are many different circuits known, that can implement this function, after analysis the sample and hold architecture has been chosen. This solution is very simple and was expected to produce good results. The schematic showing used architecture is presented in Figure 4.

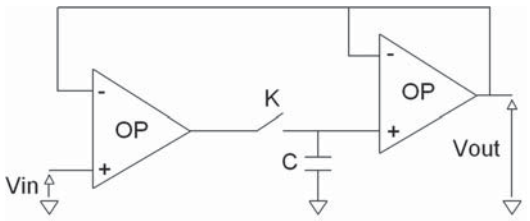

Fig. 4. Sample and hold circuit

Sample and hold circuit samples input square wave during its positive half-period and hold the value of this signal amplitude. Both the operational amplifiers are in voltage follower configuration, but they have common feedback loop. This provides low offset voltage on the output of the circuit. There are two modes of operation: sample mode and hold mode. In first of them the switch-key is closed and the input voltage is being stored in capacitor C and appears on the output. In the hold mode the switch-key is open and the capacitor is disconnected from the input buffer. Voltage stored in capacitor in previous mode is now held at the output. It is necessary to take care about the stability of the input follower during the hold mode - the key is open and the feedback loop of the input amplifier is cut. It can be fixed by adding extra switch-keys, which close the feedback loop of the input buffer.

The sample and hold architecture of demodulator requires additional control signal (sample signal) being in correlation with control signal of the modulator. It was decided to generate both these signals externally rather than place such source of interferences (another switching circuits) inside the chip.

III. Readout Circuit

This section describes details related to readout circuit design. First, the architectures of folded cascode amplifier, fully differential amplifier, VCA and PGA are presented. Then all three versions of chopper amplifier are discussed. The last subsection concerns layout design.

A. Folded Cascode Amplifier

The basic operational amplifier architecture, used to build some more complicated structures, is based on folded cascode circuit. This one - in comparison with other amplifier architectures - provides higher gain, wider input voltage range, minimization of Miller effect for gate-drain capacity in input transistors, and also can operate with lower supply voltage than another circuit solutions. The schematic of designed cascode circuit is shown in Figure 5 (see next page).

In this circuit high precision current mirrors with four transistors have been used. High current matching in active load provides high gain.

As mentioned in II-B, a special circuit called *double_cascode* has been designed to achieve minimization of input offset voltages.

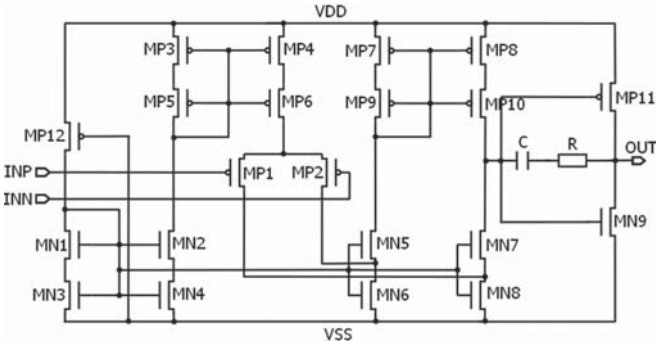

Fig. 5. Folded cascode circuit

B. Fully Differential Amplifier

The fully differential amplifier is a device with symmetrical input and symmetrical output. This type of amplifier requires additional circuit called Common Mode Feedback (CMFB), which controls the common mode voltage on its outputs. In single-ended operational amplifier applications the negative feedback (by connecting output to the negative input) is used and it determines dc offset (differential voltage towards ground) on the output. If device has two outputs, the common mode voltage also must be determined and this task is carried out by CMFB. Functional diagram of CMFB is shown at the top of Figure 6.

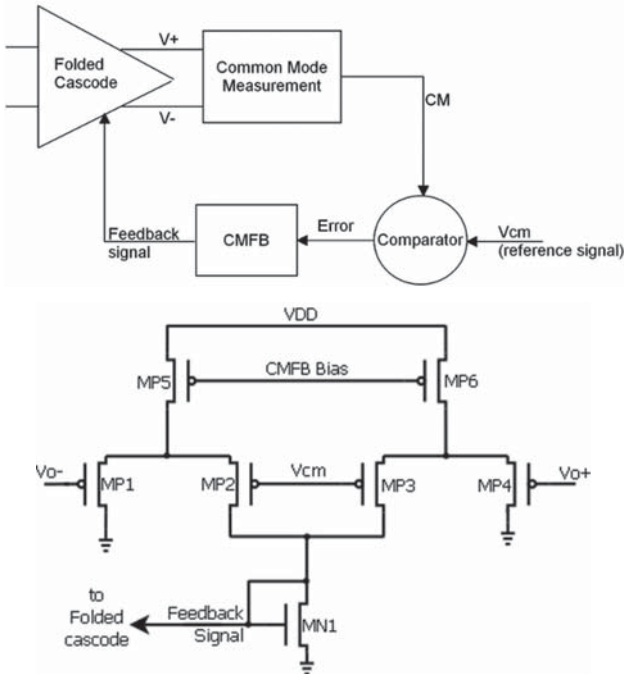

Fig. 6. Common Mode Feedback: (top) Functional diagram; (bottom) Used schematic

The CMFB circuit performs three tasks: measurement of the common mode voltage, its comparison with the reference voltage and generation of the feedback signal which controls the amplifier. Used amplifier is a folded cascode circuit (described above) with two outputs, schematic of CMFB is shown at the bottom of Figure 6. This circuit bases on a dual differential configuration, with a diode connected NMOS providing the common mode control voltage to the folded cascode circuit. With MP1-MP4 transistors matched, the current summed through MN1 is proportional to the difference between the output voltages Vo+, Vo- and the reference voltage Vcm set externally by a bias circuit. The feedback signal is used to bias the MN5-MN6 and MN7-MN8 transistors at the bottom of the folded cascode stage (see Figure 5). It is worth to notice that each stage of the amplifier needs CMFB, so circuit shown in Figure 6 is also used to bias MP11 transistor in the output stage of the folded cascode.

C. Voltage Controlled Amplifier

As it was mentioned previously (in II-B), the VCA circuit is an amplifier, with gain controlled in continuous manner by an analog signal. Usually the linear relation between the control signal and gain settings is desired. Architecture of the VCA block being the part of the designed IC is based on a simple PMOS differential pair with resistive load and the relation between gain of this circuit and transistors drain current. The idea is shown in Figure 7.

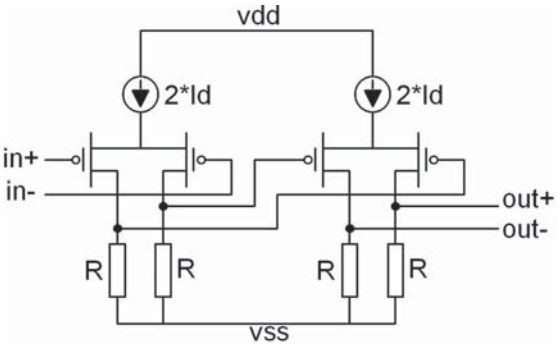

Fig. 7. The idea of VCA

The differential gain of a single PMOS pair (in saturation region) with two resistors is proportional to square root of drain current, so - to achieve linear relation - combination of two differential pairs has to be used (Figure 7).

To keep the transistors in saturation region it is required to limit the changes of drain currents to the proper range. Needed current source can be implemented using current mirror structure as it was shown in folded cascode (Figure 5). In the VCA circuit a resistive load is used intentionally instead of an active load. The gain of this circuit must be very low (0 dB - 20 dB range) and it can not be achieved using active load. It is also important to notice that change of drain current causes DC voltage change on the outputs. As long as the range of this changes is acceptable by the next stage, architecture presented in Figure 7 is sufficient.

D. Programmable Gain Amplifier

As it was described in (II-B), the PGA is an amplifier with gain controlled by external digital signals. This can be achieved using an instrumentation amplifier architecture (shown in Figure 3) with switched R1 resistor. Change of R1 influences the circuit gain according to relation (1). Modified instrumentation amplifier structure is shown in Figure 8 (next page).

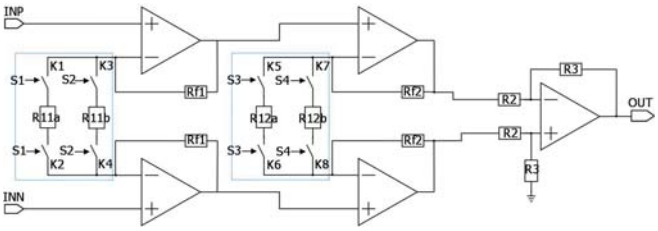

Fig. 8. Modified architecture of instrumentation amplifier

Depending on the S1/S2/S3/S4 control signals the R11a/R11b/R12a/R12b resistors are attached to feedback loops, what causes the gain to be equal to 100/1000/10000 (20/40/60/80 [dB]) respectively.

E. Designed Versions of Chopper Amplifier

According to information presented previously in III, three different versions of chopper amplifier have been designed. The difference between them concerns the AC amplifier architecture. The remaining blocks (modulator and demodulator) are exactly the same in all three circuits. First version of AC amplifier is shown in Figure 9.

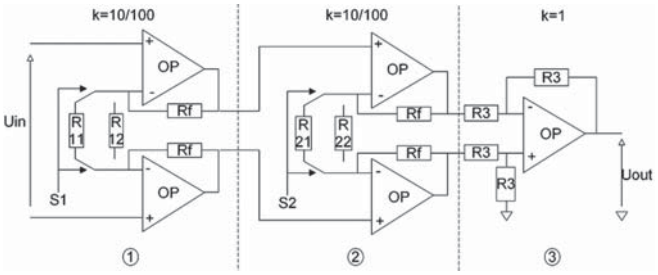

Fig. 9. The first AC amplifier circuit

It is based on architecture presented in II-B, where the resistors in feedback loops can be switched. By means of control signals, gain of this circuit can be set to 100/1000/10000.

Second version of the AC amplifier is presented in Figure 10.

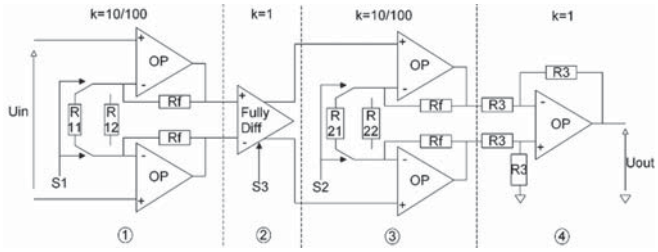

Fig. 10. The second AC amplifier circuit

It is very similar to the previous one, except that the fully differential amplifier has been placed in between fixed gain stages. This provides the ability to control common mode voltage after the first gain stage (by means of signal S3 - see III-B) to avoid saturation of devices in next circuit stages. In this way the influence of process variations and the interferences to the offset voltage can be compensated.

The last, third version of the AC amplifier is shown in Figure 11.

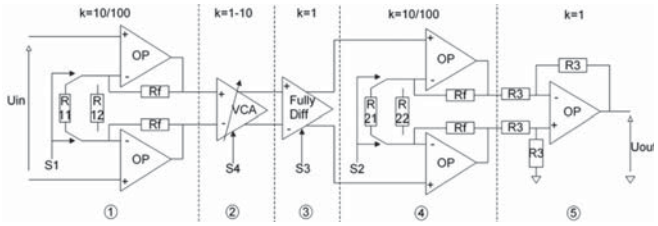

Fig. 11. The third AC amplifier circuit

In respect to the previous one, the VCA circuit has been added. This enables linear gain control in 1-10 range using signal S4, hence, the available range of gain in this circuit is 100-100000 (40 dB - 100 dB). In this circuit the fully differential amplifier performs an additional function - it cancels the VCA disadvantage concerning the relation between output DC component and gain settings (mentioned in III-C).

F. Chip Layout

In this design the commonly-known layout techniques have been utilized to achieve high immunity to interference and low susceptibility to process variations. Multifinger transistors, dummy structures, common-centroid configurations have been used in order to maximize device matching. To avoid substrate coupling [10] special guard rings have been applied. The readout circuits are fully covered by the fourth metal layer, playing the role of shielding from RF interferences as well as THz radiation. To minimize the switching noise propagation by supply lines the power-cut technique has been also applied.

Figure 12 presents the layout view of designed IC (dimensions: 2.64 x 2.64 mm).

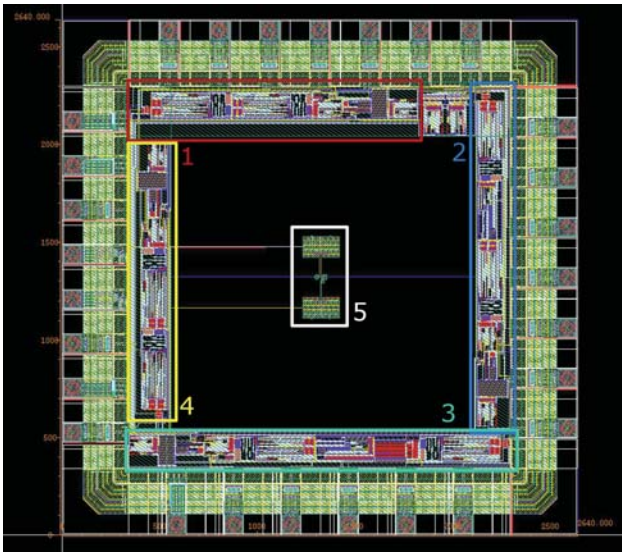

Fig. 12. Chip layout

The circuit components are marked in this figure with following numbers: 1 - chopper amplifier with first version of the AC amplifier, 2 - chopper amplifier with second version of the AC amplifier, 3 - chopper amplifier with third version of the AC amplifier, 4 - chopper amplifier with first version of the AC amplifier, connected to the detector circuit, 5 - the detector circuit (see section IV).

IV. On-chip THz Detector Circuit

The prototype IC was intended to be manufactured using regular MPW run of AMS C35B4 process [11]. Since the area of silicon consumed by discussed circuits together with I/O cells and the ring is significantly lower than minimum payable area in chosen run, it was decided to use the rest of silicon area to place on the chip another readout circuitry (fourth one) connected with detecting transistor equipped with antenna. The fourth readout circuit itself is a simple copy of the first variant discussed previously - as simplest and most reliable one. Due to the lack of any previous experiences concerning development of detecting circuits in chosen AMS process - on the one hand, and higher area cost of testing some collection of antennas - on the other, design of such an receiving circuit was based on extrapolation of previously examined solutions from ITE proprietary silicon process. Among all sets of NMOS + antenna one was chosen, providing maximum signal. The shape of receiving antenna was transferred in one-to-one scale, but in opposite to original solution it was created using all the four available metal layers, connected together by the via arrays. Taking into account that thickness of isolation between metalization levels in the IC is lower than THz wave length, such "sandwich structure" can be considered as single, thicker layer. To satisfy the design rule for maximum width of metal layers it was necessary to cut them with the sets of parallel slots of dimensions non visible for the THz wave. Moreover, slots in odd and even metal layers were distributed alternately. The rules of maximum slot length were satisfied by placing metal bridges within them. Another important issue was the choice of detecting transistor. During previous experiments it was observed, that maximum signal is yielded from FETs of moderate dimensions, close to process minimum, that's why it was not suitable to transfer detecting NMOS one-to-one from silicon process of nearly ten times larger feature size. On the other hand, the minimum transistor would be very hard to attach to the receiving antenna structure without narrowing the original metal paths, resulting in large parasitic inductance. Basing on these facts the NMOS of $w = 5\ \mu m$ and $l = 1.2\ \mu m$ was chosen as optimum, moreover allowing the metal path of minimum width to be placed above its gate and contacted to the polysilicon from both sides.

V. Prototypes Measurement

A. Application Board

The application board, shown in Figure 13 (top) was dedicated to prototypes measurement. It was *a priori* anticipated that due to the small input signals fed to IC under test special attention must be paid to shielding, the supply lines decoupling and external interferences elimination in the application board. First, the board is supplied from 12 V/7.5 Ah rechargeable battery instead of typical power supply. The target IC supply of 3.3 V and the virtual ground potential are produced at the board level using linear regulators, for the second voltage (1.65 V) made from 3.3 V the LDO regulator IC is applied. In similar way, at the board level, the clock signals for modulator and demodulator are produced. The ICL8038 integrated signal generator and two 4047 monostable multivibrators are used for that purpose, fully satisfying non restrictive requirements for those two signals. The 1.2 V from another, small battery is fed to the input dividers attached to the IC under test. The DIP-switch with pull-up resistors used for gain selection, potentiometers for input signal and VCA control, test socket and decoupling capacitors are remaining components of application board. Using the battery supply and on-board generators, it was possible to reduce the number of connections to line-powered devices to the single one - oscilloscope.

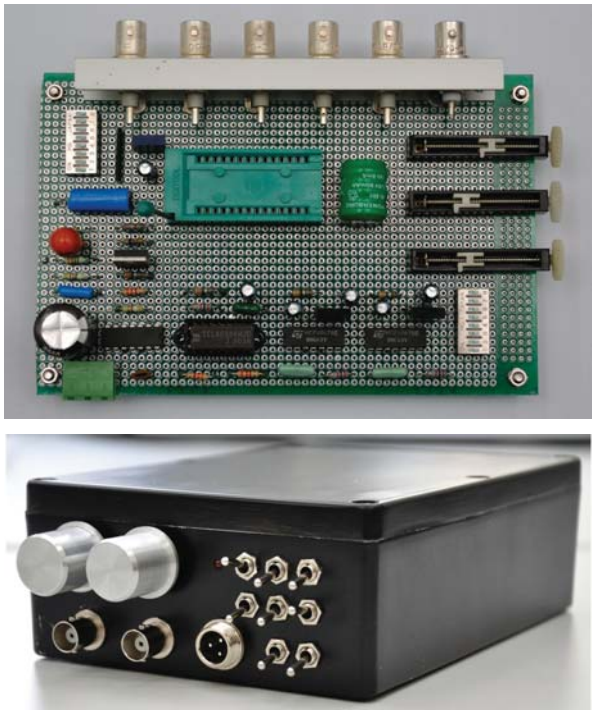

Fig. 13. Designed application board for prototypes characterization: (top) universal board with components (first version); (bottom) metal enclosure with external terminals (later version)

The next important issue was careful shielding of the IC under test, input signal dividers and switches to prevent them from working as receiving antenna. The mentioned 1.2 V battery and resistive divider were used to test the prototype IC with minimum gain setting. For the higher gains it was necessary to provide the low-noise, stable and furthermore adjustable source of DC signal ranging from tens of μV to several mV. The typical value of the output voltage from precise voltage reference IC is 1.25, 2.5 or even 5.0 V, the same concerns typical battery cells. The resistive voltage divider applied to decrease it to some hundreds of μV would require large value of one of its components, what in turn would negatively influence the noise parameters of such reference voltage source. The next issue is ability of adjusting (ideally- in linear way) the reference voltage - needed to examine the linearity or testing the VCA. In discussed experiment, both problems were overcame by non-typical application of thermocouples. Two thermocouples connected in series in opposite polarity are used to produce the output voltage proportional to the difference of their temperatures. The proportionality coefficient (Seebeck constant) is in order

of tens μV. In proposed solution one thermocouple is attached to the heatsink (large mass - thermal capacitance) heated up by two power resistors, while the second one is kept in constant temperature. At the beginning of experiments it was intended to put the second junction into thermostat but measurements shown that placing it in large amount of silicon oil in air-conditioned room is fair enough. The thermocouples leads are connected together inside the metal box, where the auxiliary voltage divider (made of special low-noise, precise resistors) can be installed to decrease the voltage for measurements with maximum gain setting. Decoupling capacitor can be also attached there. All the connections of described circuit (thermocouples leads and wiring to the board) are made as shielded ones. Without any voltage divider the internal resistance of such a non-typical measurement signal source is approx. 40 Ω and the output voltage range is from the tens of μV to approx. 60 mV. It is worth to notice that this signal source also provides the galvanic separation between output (thermocouples) and control circuitry, what is also important for interferences elimination. Measurement results proved the usefulness of presented reference voltage source concept.

During the first chip tests it turned out that demodulator circuits (see II-C) oscillate when they are loaded by moderate capacitance, i.e. cable and even oscilloscope probe capacitance. Proper circuit operation was achieved by addition of external buffers to provide cable capacitance decoupling. Modification of the demodulator block is undoubtedly one of the issues that should be addressed in next version of design.

Figure 13 (bottom) shows the application board within the shielding enclosure. Enclosure is equipped with external terminals - BNC sockets, switches and potentiometers.

B. Measurement Results

As it was mentioned in previous section (V-A), external voltage followers were added at the PCB level to buffer the demodulator output. It turned out that even in this configuration this circuit has a tendency to oscillate when the output signal amplitude is close to its upper limit. It was assumed that analyzing the input signal of demodulator (by means of auxiliary, test outputs of the IC) is more reliable. This is a square wave with k*a amplitude as it was shown in Figure 1.

If the amplifier works properly, square wave with amplitude equal to amplified input signal should be observed. In Figures 14 - 16 exemplary oscillograms are shown.

Figure 14 presents square wave for the 0.32 mV input voltage and gain set to 100/1000. Amplitude of AC signal meets the expectations but some noise is present. Probably these are interferences coming from the outside of the test setup (e. g. power net, other devices) or generated inside (clocking signals for modulator/demodulator) received and amplified by the IC under test.

Figure 15 shows common mode voltage control described in III-E. Depending on *vcm* signal, CM voltage for PGA input signals assumed different values. This mechanism constitutes protection against amplifier saturation.

Figure 16 presents linear gain control in chopper amplifier III. Depending on the *vca* signal, gain of the VCA can

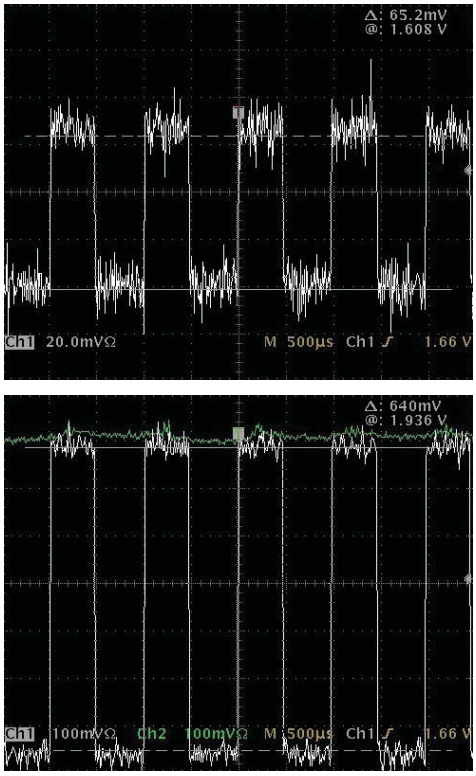

Fig. 14. Chopper amplifier I: (top) input voltage=0.32 mV, k =100, square wave amplitude =32.6 mV; (bottom) input voltage =0.32 mV, k =1000, square wave amplitude=320 mV

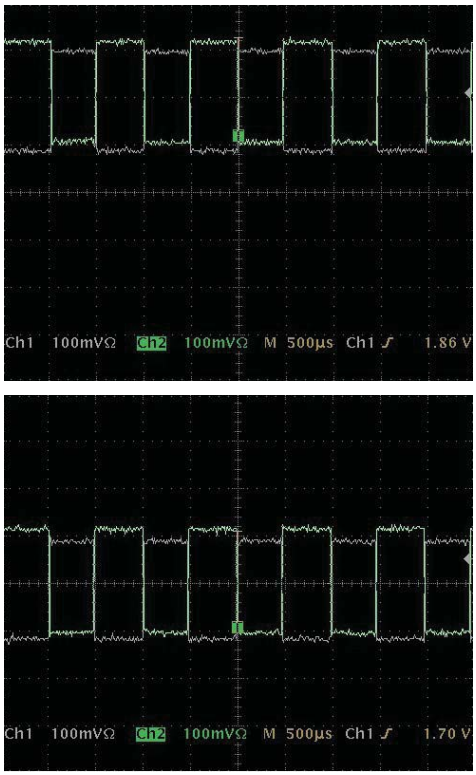

Fig. 15. Chopper amplifier II: (top) common mode voltage control, *vcm*=1.233 V; (bottom) common mode voltage control, *vcm*=1.395 V

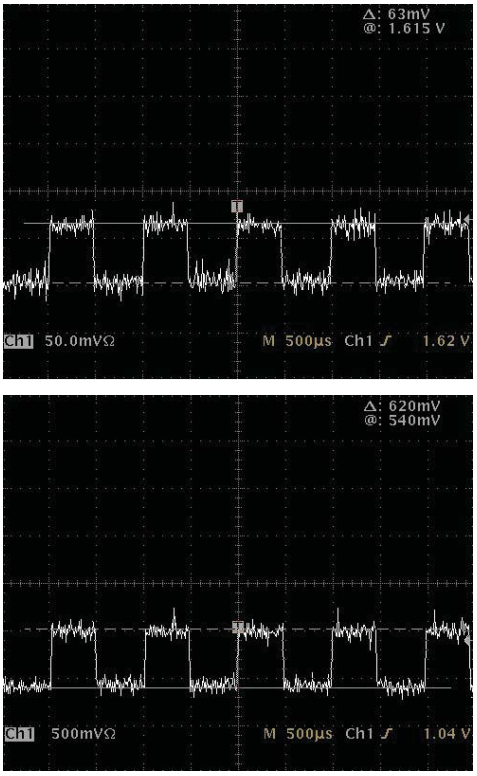

Fig. 16. Chopper amplifier III: (top) linear gain control, *vca*=1.692 V => k=100; (bottom) linear gain control, *vca*=0.2292 V => k=1000

be controlled in 1-10 range. In these figures also unwanted phenomenon can be observed - high DC offset on circuit output. It is directly connected with an undesirable component in equation (4). This offset is different for different chips, so it must be result of process variations. This proves that used layout techniques for mismatch minimization in some cases were insufficient. This definitely should be fixed in the next version of readout circuit.

C. Measurements with THz source

In the previous section the set of measurements aiming at precise characterization of the developed IC was described in details. This part of the paper deals with another set of studies - tests with THz detector and THz signal source, that means, in environment close to target application for described IC. The tests were carried out at the Institute of Optoelectronics of the Warsaw Military University of Technology. The very specific character of measurements required another test board to be build in a form of complete device. To provide proper shielding and compact mechanical structure to fit into optical lane, the aluminum alloy casting was used as an enclosure of the device. To eliminate the possible interferences coming from power line, the battery supply was used and the set of four Li-Ion cells was placed at the bottom of the enclosure. Above it, the rectangular plate is fixed being the mechanical basis for two PCBs located one above the other and connected via multipin connector. The lower PCB contains the generators of two clocking signals - for modulator and demodulator, as well as linear regulators for three supplies : the main one of 3.3V, the virtual GND of 1.65V and 5V for output buffers. All the connections to elements located at the sides of device enclosure (BNC sockets for output signals, switches for setting the gain and selecting the output signals, potentiometer) as well as to batteries are routed to this lower PCB. In this way, the upper PCB can be easily dismounted and replaced to examine different variants of amplifier-detector circuit, requiring different connections and external components. There is an 8 mm diameter hole in the cover of the enclosure, needed to allow the THz beam to achieve the detector. The surface around this hole is covered with the conductive ESD protective foam, to suppress any interferences of THz wave, which are very probable in the measurement setup, taking into account the wavelength in a range of parts of mm. Experiments were started with the readout circuit variant connected with on-chip THz detector described in section IV. Unfortunately, the response of this circuit, even with minimum gain settings, was dominated by excessive noise signal. This is caused by the RF interferences received by detecting circuitry and also thermal noise of the detector amplified by high impedance gain stages. The NMOS FET operating as detector, biased below the Vth constitutes the relatively high impedance, what allows any interferences received in its connections (including THz antenna) to be passed to the amplifier. Furthermore, the test board can not be entirely shielded because of the opening needed to direct the THz beam to the detector. It was proven, that setting the gate voltage of detecting NMOS above its Vth dramatically reduces the output noise level, because of decreasing the channel impedance, what suppresses the received interferences, but also suppresses the P-V effect caused by THz radiation.

In the second approach external NMOS-based THz detector assembled in DIL14 package, manufactured in ITE proprietary CMOS process during the former project, was connected at the PCB level to the first variant of an amplifier (PGA) from the IC under test. In Figure 17 (see next page) measurement results are shown for the detector exposed for THz beam and one covered with a blade, respectively.

Having in mind results from previous experiment, the input impedance of the readout amplifier was decreased for higher frequency range by applying the bypass capacitor. The output signals shown in the Figure 17 are taken after the second stage of the amplifier, via diagnostic outputs of the designed IC. The difference in output response of the ”dark” (right) and irradiated (left) detector can be easily noticed, but the signal to noise ratio (approx. 53dB) needs to be improved. The final experiment with this test setup was performed for the third amplifier variant (presented in III-E) - one with the VCA put after two fixed-gain stages.

Its results are shown Table I (next page). The gate-source voltage of detecting NMOS FET was set to 1.623 V which is close to its threshold voltage. The linear gain regulation is achieved by changing the VCA control signal. This table describes two extreme corners: the voltage control signal equal to 0.162 V (VCA gain is set to 1) and with voltage control signal equal to -0.814 V (VCA gain is set to 10 - its upper limit).

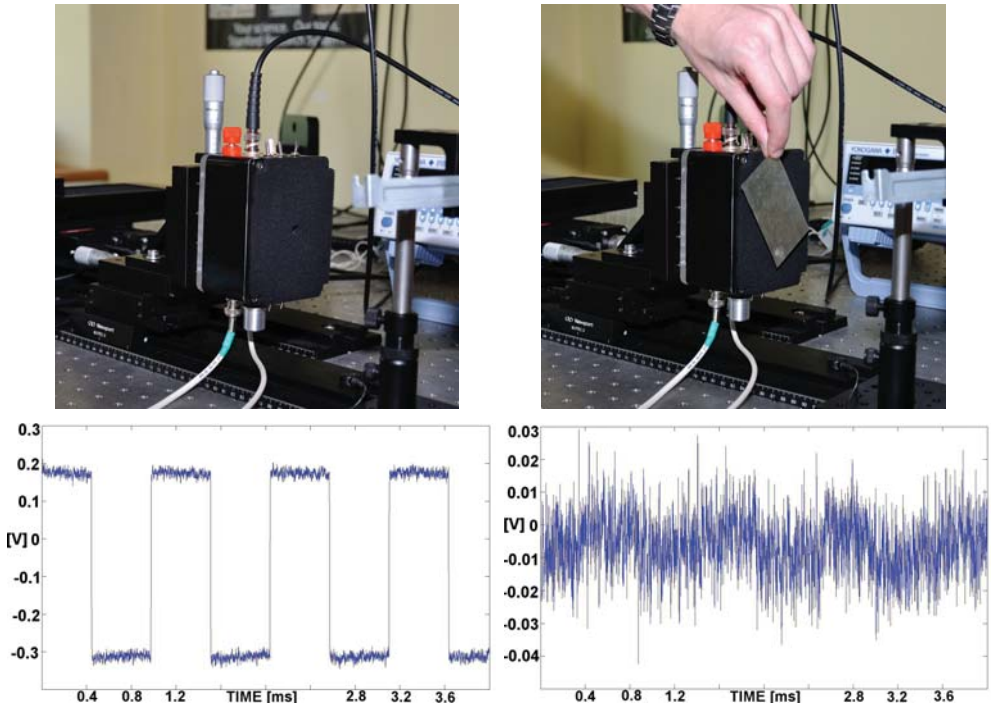

Fig. 17. (top) The application board used for THz measurement; (bottom) The output signal after the second gain stage for irradiated and covered detector (note different scale)

TABLE I
VCA MEASUREMENT

Detector Gate Voltage	VCA Control Voltage	VCA Gain	Total Gain
1.263 V	0.162 V	1	10 000
1.263 V	-0.814 V	10	100 000

D. The selective AC amplifier

The prototype ICs characterization as well as their tests in target application proved that chopper amplifier concept was the right choice for THz detector readout circuit. However, mentioned design suffered from the relatively large output noise level. Basing on the measurement results discussed in previous sections it was decided to spend additional effort to address this problem. It was identified, that the most promising filed of improvements is the AC amplifier placed in between the modulator and demodulator blocks. In the readout IC presented before, all the three versions of this block have a flat transfer curve in a range from DC to approx. 2 MHz. Since the response of irradiated NMOS FET operating as detector is a DC voltage, then the useful information after the modulation process is carried only by signal components of the switching (modulation) frequency and a few of its harmonics.That is why the low-side and high-side bandwidth limitation should result in elimination of a significant portion of unwanted signals (i.e. amplified interferences from the input, noise signal of the amplifiers) and thus, improvement of the noise parameters of the entire chopper amplifier circuitry. Figure 18 (see next page) presents the architecture of such modified structure, the theory of this improvements is given below.

At the circuit input, DC signal with the magnitude *A* and single frequency component in $f = 0$ is applied to the modulator block. As a result of modulation, its spectrum is convoluted with a square wave spectrum and produced signal, with trigonometric Fourier series expansion given by equation (5).

$$U_m(t) = \sum_{l=1}^{\infty} \frac{2A(1-(-1)^l)}{l\pi} \sin(l\pi t) \tag{5}$$

Modulated signal is then applied to the AC selective amplifier. In perfect, theoretical situation, only the frequency component $f = f_c$ is amplified (with *k* gain), the other ones are entirely suppressed.

Demodulation process is made by a circuit similar to the modulator (it is also built of CMOS switches), but this time the square wave is convoluted with a sine signal (not a DC one). As a result of this operation, a rectified sine wave is produced, with trigonometric Fourier series expansion given by (6).

$$U_d(t) = \frac{8kA}{\pi^2} - \sum_{l=2,4,6\ldots}^{\infty} \frac{16kA}{\pi^2(l^2-1)} \cos(l\pi t) \tag{6}$$

Then, the LP filter with cut-off frequency $f_o << f_c$ passes only the DC component of this rectified signal.

At the end, output wave is a DC signal with $\frac{8A}{\pi^2}k \simeq 0,81Ak$ magnitude, where *A* is an input magnitude and *k* is the gain of the AC amplifier for f_c frequency.

As a proof of this general concept, another application board was designed, in similar way as one used for measurements

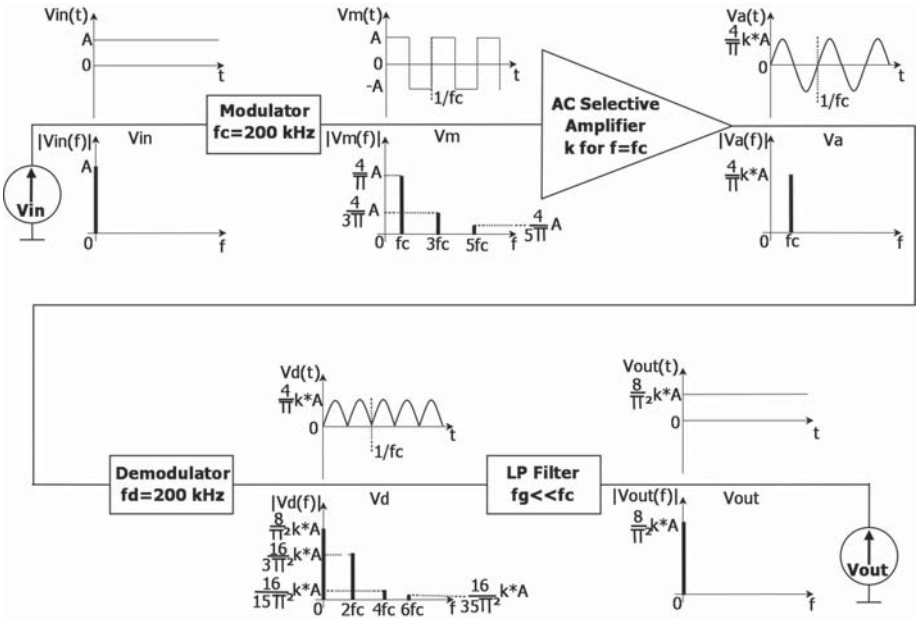

Fig. 18. Improved architecture of designed chopper amplifier with signals in time and frequency domains

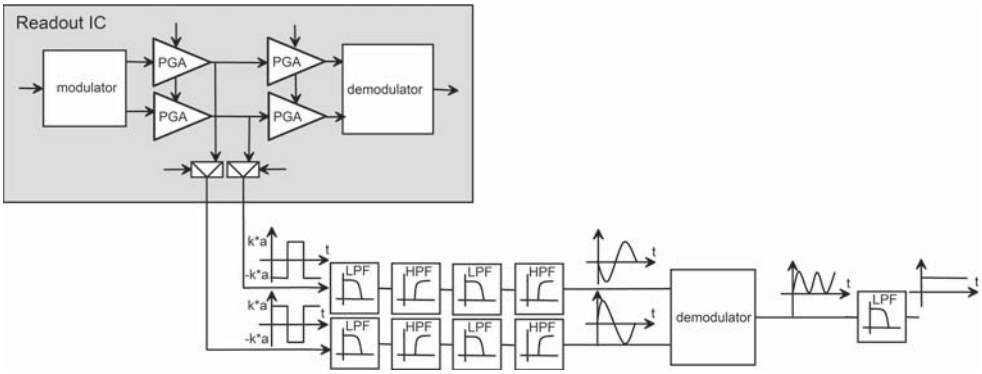

Fig. 19. The schematic view of the chopper circuit with selective AC amplifier, based on the designed IC

with THz source. It was decided to use internal blocks of previously designed readout IC and extend it with some components at the PCB level, rather than build the entire circuit starting from scratch. The auxiliary test outputs, originally intended for observation of the IC internals behavior, were utilized to output the modulated signals (complementary ones) just after they traversed the first gain stage. At the PCB level two sections of LP and HP active filters were used for shaping the AC characteristics in a manner to pass the fundamental frequency of the modulator and up to its third harmonics - in this experiment the band is wider than in previously presented calculations. Demodulation process, as it was announced, is performed at the PCB level using the CMOS switches. The complementary outputs of the demodulator are subtracted, the remaining components of the switching frequency are eliminated by an LP filter, and resulting DC signal is buffered and sent to the output. The concept of measurements with selective AC amplifier built of the designed readout IC and some off-the-shelf component is shown in Figure 19.

On account of the fact, that the selective AC amplifier concept is anticipated to be used in a next version of readout IC, the switching frequency (modulation and demodulation) was increased to 200 kHz, what guarantees, that values of all passive components (especially capacitors) can be easily implemented inside monolithic IC. As a basis for the signal path built at the PCB level the low-noise, low offset operational amplifiers from Microchip were used. The PCBs were designed with a special attention payed to the signal path and ground planes routing, as well as local separation and careful decoupling of the supply lines for noisy components. Figure 20 shows the measurement setup for testing the readout circuit based on selective AC amplifier.

VI. Conclusion

The measurements show that chopper amplifier architecture was the right choice for the IC design. The only problems concern demodulator circuit, what needs external buffering to drive capacitive load. This certainly will be addressed in

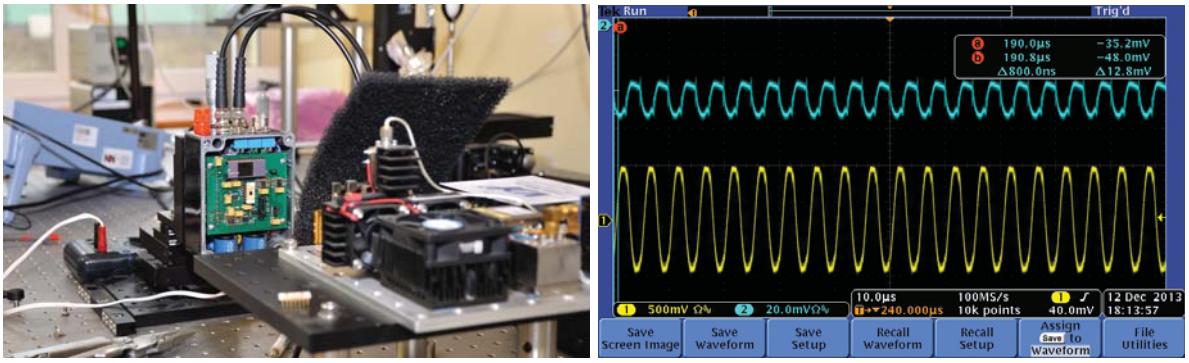

Fig. 20. (left) The measurement setup for testing the readout circuit with selective AC amplifier, the top cover removed, (right) Modulated signal after the 1st gain stage and after the selective amplifier.

the next version of design. The tests performed with the THz detector and the THz source fully proved the suitability of designed chip for target application.

The concept of selective AC amplifier, also tested with positive results regarding the signal-to-noise ratio, will be applied in the next version of the integrated readout circuit.

ACKNOWLEDGMENTS

This work was partially supported by the National Centre for Research and Development (NCBiR) within the project THzOnLine - PBS1/A9/11/2012 (full title: Multi-pixel detector for THz radiation based on selective MOS transistors and its application in biology, medicine and security systems).

REFERENCES

[1] D. Veksler, F. Teppe, A. Dmitriev, V. Y. Kachorovskii, W. Knap, and M. Shur, "Detection of terahertz radiation in gated two-dimensional structures governed by dc current," *Physical Review B*, vol. 73, no. 12, p. 125328, 2006.

[2] E. Ojefors, N. Baktash, Y. Zhao, R. Hadi, H. Sherry, and U. R. Pfeiffer, "Terahertz imaging detectors in a 65-nm CMOS SOI technology," in *ESSCIRC, 2010 Proceedings of the*. IEEE, 2010, pp. 486–489.

[3] S. Boppel, A. Lisauskas, V. Krozer, and H. Roskos, "Performance and performance variations of sub-1 THz detectors fabricated with 0.15 μm CMOS foundry process," *Electronics Letters*, vol. 47, no. 11, pp. 661–662, 2011.

[4] M. Dyakonov and M. Shur, "Shallow water analogy for a ballistic field effect transistor: New mechanism of plasma wave generation by dc current," *Physical review letters*, vol. 71, no. 15, p. 2465, 1993.

[5] S. Preu, S. Kim, R. Verma, P. Burke, M. Sherwin, and A. Gossard, "An improved model for non-resonant terahertz detection in field-effect transistors," *Journal of Applied Physics*, vol. 111, no. 2, p. 024502, 2012.

[6] J. Lusakowski, M. Bialek, D. Yavorskiy, J. Marczewski, P. Kopyt, W. Gwarek, W. Knap, K. Kucharski, M. Grodner, M. Gorska *et al.*, "Planar antennas for detection of 340 GHz band with single Si metal-oxide-semiconductor field-effect transistors," in *Infrared, Millimeter and Terahertz Waves (IRMMW-THz), 2011 36th International Conference on*. IEEE, 2011, pp. 1–2.

[7] D. Yavorskiy, J. Marczewski, K. Kucharski, P. Kopyt, W. Gwarek, M. Ratajczyk, W. Knap, B. Piętka, and J. Łusakowski, "THz Scanner Based on Planar Antenna-Supplied Silicon Field-Effect Transistors," *Photonics Letters of Poland*, vol. 4, no. 3, pp. pp–100, 2012.

[8] W. Knap, M. Dyakonov, D. Coquillat, F. Teppe, N. Dyakonova, J. Łusakowski, K. Karpierz, M. Sakowicz, G. Valusis, D. Seliuta *et al.*, "Field effect transistors for terahertz detection: physics and first imaging applications," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 30, no. 12, pp. 1319–1337, 2009.

[9] M. Sakowicz, M. Lifshits, O. Klimenko, F. Schuster, D. Coquillat, F. Teppe, and W. Knap, "Terahertz responsivity of field effect transistors versus their static channel conductivity and loading effects," *Journal of Applied Physics*, vol. 110, no. 5, p. 054512, 2011.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits*. MHHE, 2001, ch. 12 - Introduction to switched capacitor circuits, pp. 660–665.

[11] AMS AG, "0.35μ CMOS Technology Selection Guide," http://www.ams.com/eng/Products/Full-Service-Foundry/Process-Technology/CMOS/0.35-m-CMOS-Technology-Selection-Guide, [Online; accessed 05-March-2014].

Cezary Kołaciński was born in 1988. He studied microelectronics at Warsaw University of Technology (at The Faculty of Electronics and Information Technology) and obtained his M.Sc. degree in 2013. After graduation, he joined the IC & Systems Design Department at Institute of Electron Technology as IC Design Engineer. He is also currently working towards Ph.D. degree in field of readout circuit design for nMOS-based THz detectors. His main field of interest focuses on microelectronics and design of integrated circuits, with particular emphasis on analog electrical and layout design.

Dariusz Obrębski was born in 1975. He studied electronics at Warsaw University of Technology (at The Faculty of Electronics and Information Technology) and obtained his B.Sc. and M.Sc. degrees in 1998 and 1999 respectively. In 1999 he joined the Institute of Electron Technology, the ICs and Systems design Department. His areas of interest is design of integrated circuits with special emphasis on digital circuits.

Przemysław Zagrajek was born in 1979. He studied physics at Warsaw University of Technology (at The Faculty of Applied Physics and Mathematics) and obtained his M.Sc. degree in 2004. He received the Ph.D. degree in 2012 (at Institute of Physics, Polish Academy of Sciences). His areas of interest are spintronics and physics of nanodevices. He joined the Laboratory of Terahertz Techniques in Institute of Optoelectronics, Military University of Technology, and he is currently assistant professor in this Laboratory.