Improved Single-Stage OTAs Using Differential-Folded Voltage Combiners

Rui Santos-Tavares, Edinei Santin, Rui Borrego, João Oliveira, and João Goes

***Abstract*—A new technique to enhance single-stage operational transconductance amplifiers (OTAs) is presented. Enhanced DC gain and reduced input parasitic capacitances are achieved by employing two input fully-differential voltage combiners, i.e. a combination of transistors in common-drain and common-source configurations operating as a preamplifier stage. Simulation results show that the input capacitance can be as small as 195 fF (corresponding to a 46 % reduction) while achieving a GBW of 1982 MHz (@ *CL* = 1 pF) with a PM of about 60º. The complete amplifier dissipates only 1.78 mW corresponding to a figure-of-merit (FoM) of 1115 MHz·pF/mW.**

***Index Terms*—Voltage-Combiners, Single-Stage, OTA, Common-Drain, Common-Source, DTMOS**

I. Introduction

IN present days, the trend is to incorporate complete systems in longer lasting battery-powered equipment, thus requiring low power circuits [1]. Reducing power in analog circuitry is mainly related with the energy efficiency of the amplifiers (OTAs) used in the different blocks employed in the analog signal processing chain.

Single-stage amplifiers are, commonly, more power efficient and cascoding could be used to achieve higher gains. This approach, however, leads to lower output swings (OS) due to the transistors stack and supply voltage reduction. Maintaining high DC gain but also requiring high OS leads to the natural choice of using a two-stage amplifier applying cascoding techniques only in the first stage. In contrast, single-stage amplifiers do not require compensation, which represents one less design variable. In two-stage amplifiers, if proper compensation is not used, 20 to 50% of power efficiency may be lost [2]. However, through proper optimization, several practical examples [6] of two-stage amplifiers prove the contrary. An additional requirement is to achieve high gain-bandwidth product, GBW. For single-stage amplifiers, the GBW is given by $GBW(I) \approx gm(I)/CL$, where gm represents the transconductance of the differential pair, CL, the load capacitance, and I the bias current of the differential pair. In a two-stage opamp, the GBW is given by $GBW(I) \approx gm_1(I)/Cc$, where gm_1 represents the transconductance of the input stage differential pair, Cc, the compensation capacitance, and I the current of the input stage. To achieve an equivalent GBW value in a single-stage amplifier, considering that $Cc < CL$, higher transconductance of the differential pair transistors is required. Larger transistors at the input represent higher input parasitic capacitance, Cpi, which degrades the feedback factor, β, when single-stage amplifiers are used in closed-loop configurations.

One solution to the input parasitic capacitance problem is to use additional source follower amplifiers at the input of the amplifier [7]. In this case, the overall gain is reduced by a factor of 0.7 to 0.9 V/V resulting from the additional source follower at the input.

On other hand, designs under nanoscale technologies suffer a reduction of the transistors intrinsic gain (gm/gds) of about 20 dB, and the intrinsic gain variability rises about 10 dB [8]. Instead of using single-stage topologies, engineers tend to use multi-stage or, in alternative, positive feedback [9], feed-forward [10][11] or gain-boosting techniques[12].

The objective of this paper is to propose an improvement to the design of single-stage amplifier using, at the inputs, a fully-differential voltage combiner, i.e., a combined common-source common-drain topology. Single-stage amplifiers are less complex to size, have less stability problems and have better power efficiency. The proposed voltage combiner introduces a non-dominant pole at higher frequency, which does not interfere with the amplifier bandwidth; enhances the overall amplifier gain by a factor of 6 to 12 dB (depending on sizing); and the feedback factor in a given application will be improved due to the reduced parasitic capacitance at its inputs.

II. Proposed Idea and Circuit Description

A. Proposed idea

In the past, a single-ended source follower was used to reduce the input parasitic capacitances of the OTA [7]. In this paper, we propose to incorporate a differential voltage combiner (VCOM) stage between the inputs of the circuit and the single-stage amplifier, as shown in the block diagram of the Fig. 1 (a). This preamplifier stage reduces the input parasitics, $C_{pi} < C_{pi2}$, and enhances the overall gain. The complete DC gain expression is given by

$$A_V = A_{VCOM} \cdot A_{OTA} \quad (1)$$

where A_v is the overall gain, A_{VCOM} is the gain of the VCOM, and A_{OTA} represents the gain of the single-stage OTA.

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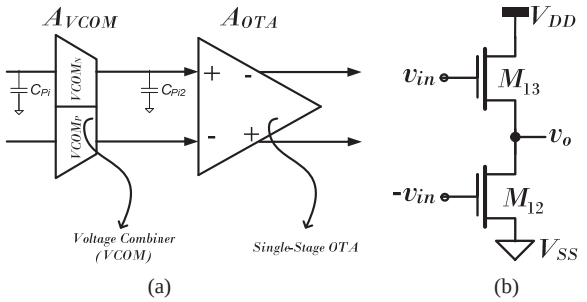

Figure 1. a) Block diagram illustrating the proposed circuit technique; b) VCOMn (NMOS VCOM) circuit conceptual idea.

The electrical circuit technique idea is depicted in Fig. 1 (b). It basically employs a combination of NMOS transistors in configuration of common-source, M_{12}, and common-drain, M_{13}. High input impedance is equally accomplished.

After simplifying the small signal equivalent (differential-mode, DM) of the VCOM and substituting the components by their Y-parameter equivalents, the behavioral signal path model [14] is extracted and illustrated in Fig. 2 (for simplicity only half the circuit is shown). This model permits large insight in the small-signal behavior of the amplifier and is a fundamental tool in the extraction of the differential gain transfer function. It is possible to verify: the Miller effect through parasitic capacitance cgd_1, the pole(s) and zero(s), and the order of the transfer function (in this case, 1st order).

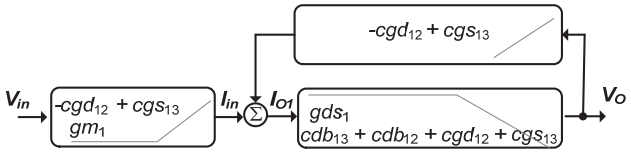

Figure 2. Behavioral signal path model of the voltage combiner stage (for simplicity only half the circuit is shown)

Using the behavioral signal path model described in Fig. 2 and writing the equations for I_{O1} and V_O, it is possible to extract the transfer function of the VCOM. For the sake of simplicity, minor simplifications were used in the derived equations:

$$gds_1 = gds_{12} + gds_{13} \tag{2}$$

$$cdb_1 = cdb_{12} + cdb_{13} \tag{3}$$

Body effect of transistors M_{12} and M_{13} were neglected, but can be easily included into the equations.

$$\mathrm{TF}_{VCOM} = \frac{gm_{12} + gm_{13} + (cgs_{13} - cgd_{12}) \cdot s}{gm_{13} + gds_1 + (cdb_1 + cgs_{13} + cgd_{12}) \cdot s} \tag{4}$$

From the transfer function it is possible to obtain the low-frequency open-loop gain (DC gain) of the VCOM stage, A_{VCOM},

$$A_{VCOM} = \frac{gm_{12} + gm_{13}}{gm_{13} + gds_1} \tag{5}$$

considering that $gm_{13} >> gds_1$, a good approximation can be given by,

$$A_{VCOM} \approx \left(1 + \frac{gm_{12}}{gm_{13}}\right), \qquad |A_{VCOM}| > 1 \tag{6}$$

Sizing the circuit to attain $gm_{13} \approx gm_{12}$, 6 dB are added in the overall DC gain of the amplifier.

Also, the dominate pole, ω_{p1VCOM}, is computed using:

$$\omega_{P1_{VCOM}} = \frac{gm_{13} + gds_1}{cdb_1 + cgs_{13} + cgd_{12}} \tag{7}$$

The gain-bandwith product (GBW) is given by

$$\mathrm{GBW}_{VCOM} = \frac{gm_{12} + gm_{13}}{cdb_1 + cgs_{13} + cgd_{12}} \tag{8}$$

The parasitic capacitance, C_{pi} is given by

$$C_{pi} = cgs_{13} + cgd_{13} + cgs_{12} + cgd_{12} \tag{9}$$

B. Circuit description

The suggested circuit for implementing a fully-differential voltage combiner block (the VCOM) is shown in Fig. 3. It is a fully-differential combined with a folded common-drain (PMOS) and common-source (NMOS) structure. The gate terminals of the PMOS transistors, M_{12}, have been short-circuited to the bulk terminal (DTMOS) [3] to dynamically reduce the body effect. Since the threshold voltage is dynamically adjusted, the input PMOS device can be sized smaller for a given V_{DS} saturation voltage (V_{DSAT}), which translates in smaller area and lower parasitic capacitances. Following the same circuit analyses shown in the previous sub-section, II-A), the DC gain (A_{VCOM}) can be approximated to

$$A_{VCOM} = \frac{gm_{13} + gm_{12} + gmb_{12}}{gm_{12} + gmb_{12} + gds_{13} + gds_{12} + gds_{11}} \tag{10}$$

Moreover, the GBW_{VCOM} is given by

$$\mathrm{GBW}_{VCOM} = \frac{gm_{13} + gm_{12} + gmb_{12}}{cdb_{13} + cgd_{13} + cgs_{12} + csb_{12} + cgd_{11} + cdb_{11}} \tag{11}$$

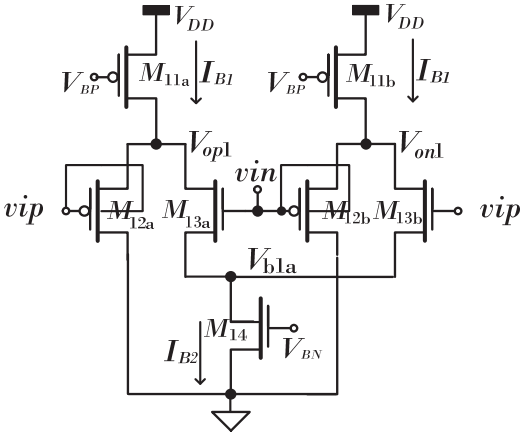

Figure 3. Proposed input fully differential voltage combiner circuit (VCOM).

C. DTMOS technique

The DTMOS technique was first introduced in 1994 [3]. Since then, many novel circuit applications of this technique have been proposed. The DTMOS technique is mostly used in digital applications in which the gate and body of the MOSFET are tied together. This reduces the leakage current during OFF state and reduces the threshold voltage during ON state to increase the overdrive voltage. It is also possible to use the DTMOS technique in bulk CMOS technology for analog circuit applications [5]. In these applications, the body terminal of the MOSFET transistor acts normally as a forth terminal.

Several issues should be considered while using the bulk as the forth terminal of the transistor. First of all, the bulk terminal has a lower transconductance, *gmb*, compared to gate transconductance, *gm*. Second, the parasitic capacitance of the bulk terminal can be larger than the parasitic capacitance of the gate terminal. This is due to the relatively larger area of the n-well/p-well in which the PMOS/NMOS transistor is formed. On other hand, connecting the bulk to the gate, the threshold voltage decreases and one can size a smaller transistor, to maintain the same V_{DSAT} voltage, decreasing the input (gate+bulk) parasitic capacitances. Moreover, applying the input signal to bulk terminal, maintaining the same transistor sizing, one can increase 20 to 30% the value of the GBW (since *gmb* adds to *gm*).

III. Design Example and Simulation Results

A. Design example

For the proof of concept, the inverter-based single-stage OTA shown in Fig. 4 is used. Also, the PMOS transistors, M_{22}, are connected in DTMOS configuration [3]. However, the proposed technique can be extended, straightforwardly, to any single-stage classic topology such as the folded-cascode, the telescopic-cascode or the mirror-cascode OTA.

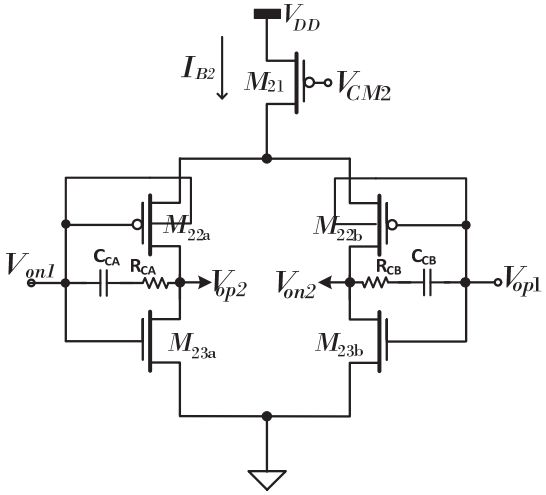

Figure 4. Proposed differential single-stage OTA used for proof of concept.

To minimize the power consumption and area, transistors widths and current in the biasing circuit are scaled down by a factor of eight with respect to the main amplifier circuit. Using the same circuit analysis methodology, as described in the previous sub-section, the DC gain of the inverter-based single-stage amplifier stage, A_{Vamp}, is given by [6]

$$A_{Vamp} = -\frac{gm_{22} + gm_{23}}{gds_{22} + gds_{23}} \tag{12}$$

To a good approximation, A_{Vamp} can be given by

$$A_{Vamp} \approx -\frac{gm_{22}}{gds_{22}} \tag{13}$$

Finally, the parasitic capacitance, C_{pi2} is given by

$$C_{pi2} = cgs_{23a,b} + cgd_{23a,b} + cgs_{22a,b} + cgd_{23a,b} + cbs_{22a,b} + cbd_{22a,b} + cc_{a,b} \tag{14}$$

Common-mode (CM) feedback (CMFB) of the single-stage is accomplished through a dedicated switched-capacitor (SC) circuit, as illustrated by Fig. 5, and the output control voltage, V_{CM2}, is given by $V_{CM2} = (V_{OP2} + V_{ON2})/2$ [13]. This control voltage biases M_{21}. Voltage V_{CM2} is connected to the main amplifier through a negative feedback loop thus reducing the effects of PVT variations on the amplifier. Voltage V_{CMI} is the DC bias voltage of PMOS M_{21}.

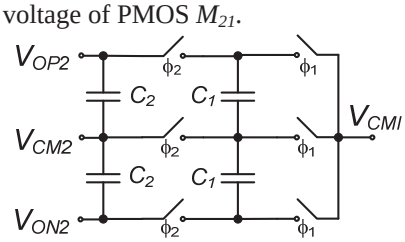

Figure 5. Common-mode feedback network for single-stage OTA (CMFB).

B. Simulation results

The circuit proposed here (the circuit shown in Fig. 1a and in which the single-stage OTA is the one shown in Fig. 4) was designed in a 130 nm high-speed CMOS technology (L_{min} = 120 nm). The mobility and threshold parameters (Level 2), K_N, K_P, V_{TN} and V_{TP} parameters of the devices are, respectively, 525 μAV^{-2}, 145 μAV^{-2}, 0.38 V and -0.33 V. For V_{CMI}, the value of 450 mV was used. The load capacitance considered, *CL*, is 1 pF, with a Miller compensation capacitance of 0.9 pF and a Miller resistance of 1 kΩ. These Miller capacitance and resistance are used to compensate/give stability to the full circuit: VCOM+OTA. The power supply of the circuit was swept in a range from 0.5 V to 1.32 V. The graphs presented next show the results of the key performance parameters of the amplifier over this wide power supply range: DC gain (Fig. 6), GBW (Fig. 7), phase margin (PM) (Fig. 8), and FoM (Fig. 9). Notice that, although the simulation results are shown for such wide range of power supply, for the target application, the OTA has been designed and optimized for an operating V_{DD} of 0.8 V ± 10%. With the supply voltage of 0.8 V, the simulated amplifier achieves a DC gain of about 58 dB. The DC gain enhancement given by the voltage combiner circuit is about 7 dB. Furthermore, the simulated GBW is 1982 MHz and the phase margin is 60º for a power dissipation of only 1.78 mW.

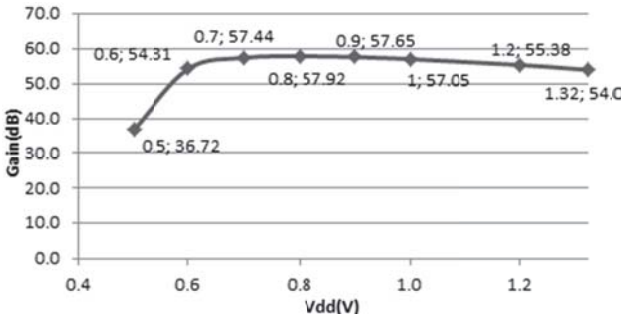

Figure 6. Gain vs. power supply.

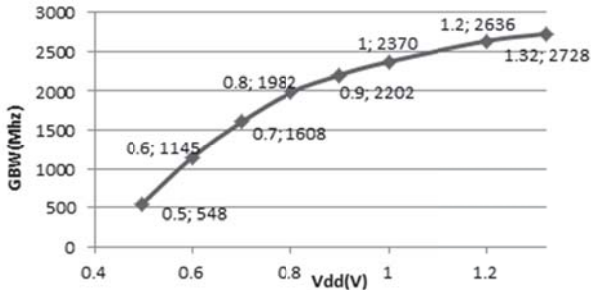

Figure 7. Gain-bandwidth product vs. power supply.

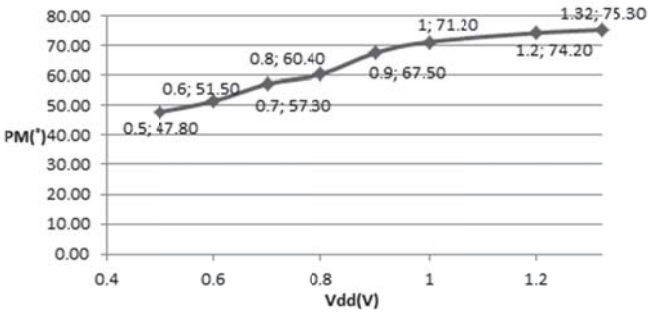

Figure 8. Phase margin vs. power supply.

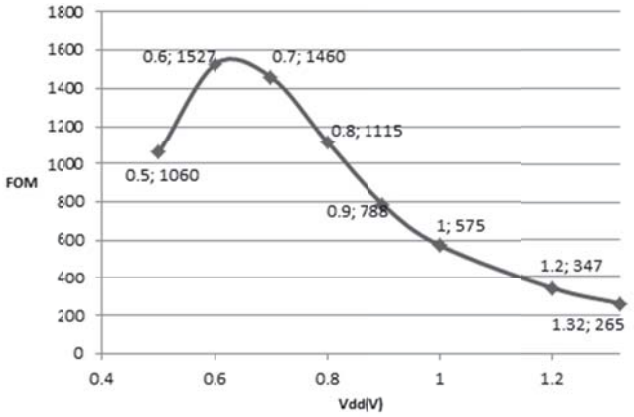

Figure 9. FoM vs. power supply.

TABLE I.
KEY SIMULATED PERFORMANCE PARAMETERS

Technology	130 nm
Supply Voltage	0.8 V
DC Gain	58 dB
GBW (@ *CL* = 1 pF)	1982 MHz
C_{pi} (see Fig. 1-a)	195fF
C_{pi2} (see Fig. 1-a)	363fF
Phase Margin	60º
Total current	2.23 mA
Power dissipated	1.78 mW
FoM	1115 MHz.pF/mW

The complete amplifier accomplishes a FoM = GBW·C_L/P [MHz·pF/mW] [15] of 1115 MHz·pF/mW. Table I presents the summary of the simulated key performance results.

IV. CONCLUSIONS

This paper described a new technique to enhance single-stage OTAs. The results showed that introducing two fully-differential voltage combiners, i.e., a combination of transistors in common-drain and common-source configurations operating as a preamplifier stage, enhance DC gain and decrease input parasitic capacitances. Simulation results also indicated that the input capacitance can be made as small as 195 fF (corresponding to a 46 % reduction, when compared to the case where the preamplifier is removed) while achieving a GBW of 1982 MHz (@ *CL* = 1 pF) with a stable response (PM=60 º). The proposed amplifier dissipates only 1.78 mW (with a 0.8 V supply) corresponding to a FoM of 1115 MHz•pF/mW.

REFERENCES

[1] R. Tavares, et al., "Design and optimization of low-voltage two-stage CMOS amplifiers with enhanced performance", ISCAS 2003, vol.1, pp. I-197-200, May 2003.

[2] Huijsing, Johan, "Operational Amplifiers: Theory and Design", Springer; 2nd edition. 2011; ISBN 9400705956.

[3] Assaderaghi, F., Sinitsky, D., Parke, S., Bokor, J., Ko, P.K., Chenming Hu "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation", IEEE Electron Devices Meeting, No. 12, Vol. 15, pp. 809-812, 1994.

[4] José Rui Custódio, Michael Figueiredo, Edinei Santin, João Goes, "A CMOS Inverter-based self-biased fully differential amplifier", in Luis M. Camarinha-Matos, Pedro Pereira, Luis Ribeiro, editors, *DoCEIS*, volume 314 of *IFIP Emerging Trends in Technological Innovation*, pp 541-548, Springer, 2010.

[5] Maymandi-Nejad, M., Sachdev, M., "DTMOS technique for low-voltage analog circuits", IEEE Transactions on Very Large Scale Integration (VLSI), Vol. 14, Issue 10, Pages 1151-1156, 2006.
[6] M. Figueiredo, et al., "A Two-Stage Fully Differential Inverter-based Self-Biased CMOS Amplifier with High Efficiency", IEEE T-CAS I: Regular Papers, Vol. 58, Issue 7, Page(s): 1591 – 1603, 2011.
[7] Won-Chul Song, et al. , "A 10-b 20-Msample/s Low-Power CMOS ADC", IEEE JSSC, Vol. 30, Issue 5, Page(s): 514 – 520, 1995.
[8] Pekarik, J. et al. , " RFCMOS Technology from 0.25um to 65nm: The State of the Art", Proceedings of the IEEE 2004 CICC, pp. 217-224, 2004.
[9] Mezyad M. Amourah and Randall L. Geiger, "All Digital Transistors High Gain Operational Amplifier Using Positive Feedback Technique", ISCAS 2002, Vol. 1, Page(s): I-701 – I-704, 2002.
[10] Rida S. Assaad and Jose Silva-Martinez, "The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier", IEEE JSSC, Vol 44, Issue 9, Page(s): 2535 – 2542, 2009.
[11] You Zheng; Saavedra, C.E., "Feedforward-Regulated Cascode OTA for Gigahertz Applications," TCAS-I: Regular Papers, vol.55, no.11, pp.3373,3382, Dec. 2008.
[12] K. Gulati, H-S. Lee, "A ±2.45V-Swing CMOS Telescopic Operational Amplifier", ISSCC 1998, Page(s): 324 – 325, 456, 1998.
[13] O. Choksi; L.R. Carley, "Analysis of switched-capacitor common-mode feedback circuit", IEEE TCAS II: Analog and Digital Signal Processing, vol.50, pp. 906-917, Dec. 2003.
[14] F. Leyn, W. Daems, G. Gielen, W. Sansen, "A behavioral signal path modeling methodology for qualitative insight in and efficient sizing of CMOS opamps", CAD, Dig. of Tech. Papers, pp. 374-381, Nov 1997.
[15] A. D. Grasso, G. Palumbo and S. Pennisi, "Three-Stage CMOS OTA for Large Capacitive Loads With Efficient Frequency Compensation Scheme", IEEE TCAS-II, Vol. 53, pp. 1044-1048, Oct. 2006.

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