Realization of Logic Integrated Circuits in VeSTIC Process - Design, Fabrication, and Characterization

Krzysztof Domański, Grzegorz Głuszko, Andrzej Sierakowski, Daniel Tomaszewski, and Dariusz Szmigiel

***Abstract*—A design and manufacturing of test structures for characterization of logic integrated circuits in a VeSTIC process developed in ITE, are described. Two variants of the VeSTIC processs have been described. A role and sources of the process variability have been discussed. The VeSFET I-V characteristics, the logic cell static characteristics, and waveforms of the 53-stage ring oscillator are presented. Basic parameters of the VeSFETs have been determined. The role of the process variability and of the parasitic elements introduced by the conservative circuit design, e.g. wide conductive lines connecting the devices in the circuits, have been discussed. Based on the inverter layout and on the process specification, the parasitic elements of the inverter equivalent circuit have been extracted. The inverter propagation times, the ring oscillator frequency, and their dependence on the supply bias have been determined.**

***Index Terms*—VeSTIC; VeSFET; logic cell, logic integrated circuit; ring oscillator; parasitic elements; oscillation frequency; compact modeling**

I. Introduction

A Vertical Slit Technology for Integrated Circuits (VeSTIC) is a method for IC manufacturing introduced in [1, 2]. The process enables fabrication of the circuits consisting of FinFET-type devices (VeSFETs, operating both in inversion and accumulation modes) [3,4], junction field-effect transistors (VeSJFETs, with poly-Si gate/Si channel junctions) [5], and bipolar transistors (VeSBJTs, having poly-Si emitters and collectors) [6]. In the ideal case the subsequent photolithography steps are based on regular grids of identical circular shapes. These shapes are patterned in different materials (silicon, polysilicon, oxide, metal). They are also used to define doping of different silicon and poly-Si areas. A comprehensive analysis of the VeSFET operation carried out using numerical simulations demonstrated promising characteristics of these devices: low OFF-state current, low subthreshold slope, satisfactory current efficiency in the ON-state, high I_{ON}/I_{OFF} ratio [7]. Additionally, if the VeSFET gates are independent, then the devices feature an additional functionality, i.e. a given gate threshold voltage control by the opposite gate. The independent gates may be obtained e.g. by a chemical mechanical planarization (CMP) step. Such an approach will be briefly mentioned in the next part of the paper.

K. Domański, G. Głuszko, A. Sierakowski, D. Tomaszewski and D. Szmigiel are with the Division of Silicon Microsystem and Nanostructure Technology, Instytut Technologii Elektronowej (ITE), Warsaw, Poland (e-mails: kdoman@ite.waw.pl, ggluszko@ite.waw.pl, asierak@ite.waw.pl)

The theoretical considerations on the VeSFET operation were partially confirmed by results of measurements of experimental devices fabricated in two laboratories [8, 9, 10]. However, it should be noted, that the architecture of these devices was significantly different from the original VeSFET concept [1, 2]. In particular, in the transistors reported in [9,10] only the channels were patterned as the narrow slits delimited by pairs of trenches of the circular shape. This approach was caused by the limitations of the available equipment for the photolithography, the parameters of which were insufficient (e.g. alignment accuracy > 250nm) for multiple patterning of dense matrix of circular shapes having the radius order of tens of nm, and for subsequent patterning of the contacts within these small areas.

Following the promising results of the VeSFET modeling and device-level characterization, attempts were made to develop methods for design of integrated circuits (ICs) in the VeSTIC technology. These works were focused not only on the modeling/simulation aspects, but first of all on a realization of functions at the circuit-level and on the routing design. Both issues are strongly affected by the device architecture and by arrangement of a given IC as a regular array of the transistors of required electrical characteristics, where the circuit functions are defined at the metallization layers. These factors disable a freedom in the device layout design, which allows to achieve different current efficiencies. Such an approach is commonly used e.g. in the standard techniques of the analog IC design. In the design of the digital CMOS ICs, differences between the carrier mobilities in the n- and p-type channels must be compensated. However, it is not possible by using wider p-type VeSFETs, as in the planar CMOS processes. Therefore, the transistors must be connected accordingly to achieve non-standard characteristics. This operation is of course quantized. Such an approach, together with the grid-like placement of the transistors entails a necessity of dedicated connections between them. In [11] such an analysis was done and solutions for the analog and digital ICs were proposed. In [12] an interesting approach towards logic cell design based on the VeSFETs with two independent gates was presented. In [13] a possible application of VeSFETs for the SRAM memories design was discussed including routing between the devices and between the SRAM cells.

In the prior works on the IC design based on the VeSTIC process only solutions of the selected design issues were presented, which were not verified experimentally. Recently, a fabrication of the test structure containing simple logic gates and integrated circuit blocks based on complementary VeSFETs was reported [14]. The discussion presented there was focused on an analysis of parasitic capacitance and resistance effects on operation of the ring oscillator (RO). It was shown that the parasitic elements determined the RO timing. The large parasitics were due to the process limitations briefly mentioned above. In this paper, we present in a more comprehensive way results of this experiment, including the test structure design, process description, measurements of the individual test devices, logic gates, and of the ring oscillators. Results of the device level measurements were partially reported elsewhere [9, 10, 15].

The paper is arranged as follows. The VeSTIC process used for fabrication of the test circuits is briefly described in the Section II. A design of the devices and circuits is described in the Section III. Results of the their measurements are presented and discussed in the Section IV. A procedure for the extraction of the parasitic elements strongly affecting the logic circuit operation is described in the Section V. A procedure for estimation of the RO frequency is described in the Section VI, whereas operation of the "ideal" oscillator is characterized in the Section VII. The Section VIII summarizes the paper.

II. VeSTIC Process

The test structures were manufactured in two different processes. Individual transistors and inverters with were made in the full technological sequence including the CMP of polysilicon layers. These VeSFETs had two independent gates at the sidewalls of the channels. More complex structures (ring oscillators and logic gates) were manufactures in the modified process without the CMP step. Those VeSFETs had continuous polysilicon gates wrapping the top surface (covered with thick silicon oxide layer) and sidewalls of the channels. The polysilicon paths were also used as the first level of electrical connections in the RO circuit. The modified technological process differed from the full process sequence also with the thickness of the polysilicon layer and the polysilicon doping process.

All types of structures were manufactured on 4-inch SOI wafers with 340 nm thick device layer and 400 nm thick buried oxide (BOX). The starting thickness of Si layer was reduced down to 190 nm due to multiple thermal oxidation, doping and wet oxide etching processes. In the first two photolithography steps the wafers were implanted with boron ($1.5 \cdot 10^{17}$ cm^{-3}) and phosphorus ($2.5 \cdot 10^{17}$ cm^{-3}) and annealed to obtain nearly uniform concentration of the dopants. We used shallow trench isolation (STI) to isolate transistors from each other. The trenches were formed by the plasma etching of 100 nm thick thermally grown SiO_2 layer and 190 nm thick Si device layer. The mechanical stress resulting from the thermal expansion mismatch between the device layer and trench filling affects the carrier mobility and the transistor performance. To reduce this effect, a low temperature plasma enhanced chemical vapor deposition (PECVD) process was used to fill the shallow trenches with SiO_2. The transistor channels were formed as narrow silicon passages (slits) between the source and drain regions. The slit and trench patterns were etched in the same process. The BOX layer was almost untreated during this process, however several nanometers might be etched in some regions as a result of extending the etching time to compensate for nonuniformity of the device layer thickness. A 12 nm thick sacrificial oxide was grown and removed by wet etching to reduce a sidewall radiation damage and a surface roughness induced by the dry-etching processes. The 7 nm gate oxide in the VeSFETs was thermally grown at 950°C. This step further reduced the width of the slit by 18 nm.

After this step two process variants were used. For manufacturing of ring oscilators and logic gates, the 350 nm thick polysilicon layer was deposited in the LPCVD process. Then, two photolithography steps followed by boron or phosphorus implantation (dose $5 \cdot 10^{15}$ cm^{-2}) formed doping suitable for p- and n-type polysilicon gates. Alternatively, the wafers containing transistors with independent polysilicon gates were processed in the longer sequence. The first layer of 500 nm thick polysilicon was deposited and after two photolithography steps, phosphorus and boron ions were implanted (dose $5 \cdot 10^{15}$ cm^{-2}). Next, additional 500 nm thick polysilicon layer was deposited and annealed. The CMP step carried out in Fraunhofer Institute for Silicon Technology (ISIT) was used to separate the polysilicon regions by removing the polysilicon layer above the Si slit and 100 nm thick SiO_2 stop layer. The wafers were polished with the colloidal-silica-based Klebosol 1508-50 slurry to remove a native silicon dioxide. Then, Planerlite 6103 slurry was used to obtain a high polish rate of the polysilicon and high polysilicon/oxide selectivity. A trench over-polish dishing was found after CMP. It was deeper for longer polishing time, especially for wider trenches. We observed that the n-type polysilicon layer was more susceptible to dishing than the p-type layer.

In both technological variants the photolithography and plasma etching steps formed final pattern of the polysilicon gates. We formed n- and p-channel VeSFET sources and drains using two photolithography steps followed by boron ($5 \cdot 10^{15}$ cm^{-2}/30 keV) or phosphorus ($5 \cdot 10^{15}$ cm^{-2}/40 keV) ion implantation. Then, a low temperature PECVD process was used to fill shallow trenches with 350 nm thick SiO_2 layer. After photolithography and plasma etching of contacts, process was completed with a single level Al:Si metallization sintered at 435°C.

III. Test Device and Circuit Design

The test structure designed for evaluation of the VeSTIC process comprised multiple devices and blocks: individual VeSFETs, logic gates, and ring oscillators. They are briefly presented in the following subsections.

A. *Individuald VeSFETs*

The individual VeSFETs of different geometries were designed for monitoring of the process quality, for validation of the concept of CMP application as means of manufacturing of the VeSFETs with two independent gates, and for assessment of the slit geometry effect on the device electrical behavior. Schematic views and SEM images of the channel regions of the individual devices with the continuous and splitted gates are shown in Fig. 1 and Fig. 2, respectively.

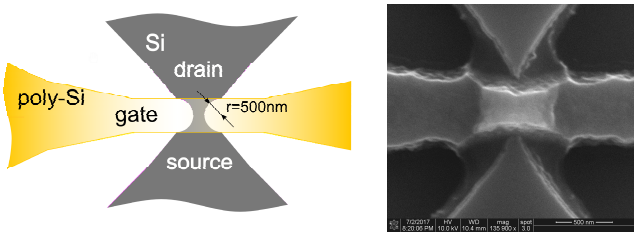


Fig. 1. A schematic view and SEM image of the VeSFET channel with the continuous poly-Si line above the slit area (after definition of the gates).

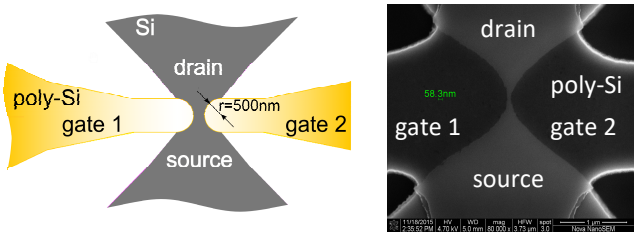


Fig. 2. A schematic view and SEM image of the VeSFET channel with two independent gates at the sidewalls of the slit (after CMP and definition of the gates).

B. *Logic gates*

Based on the complementary VeSFETs with non-splitted gates, simple logic cells were designed. The inverters, NOR and NAND gates having different architectures were included in the test structure for analysis of the substrate voltage effect on the logic cell characteristics, and for assessment of an effect of the p-channel device multiplication on the gate performances, e.g. transfer I-V characteristics, current consumption. SEM images of the NOR and NAND gates with single load p-channel VeSFETs are shown in Fig. 3, and Fig. 4. Analogous gates were designed in which there were two pVeSFETs connected in parallel, working as the loads. They are not illustrated in this work due to its larger complexity. In the images large polysilicon and metal areas are visible. Therefore a strong effect of the parasitic capacitances on the gate behavior was expected. This hypothesis has been confirmed both by the experiments and by the analysis of the gate layout presented below in a discussion of the ring oscillator operation.

C. *Ring oscillators*

The ring oscillators were included in the test structure for assessment of the overall process quality, of the switching characteristics, and of an effect of the parasitics on the gate operation. In the experiment the 53-stage ring oscillator was used. Each stage (inverter) consisted of three VeSFETs, one with n-type channel, and two with p-type channel connected in parallel.

Details of the inverter architecture are better visible in Fig. 5 showing two RO stages marked in Fig. 6, where the image of the complete RO is shown. The circuit is equipped with the buffer for the voltage waveform measurements.

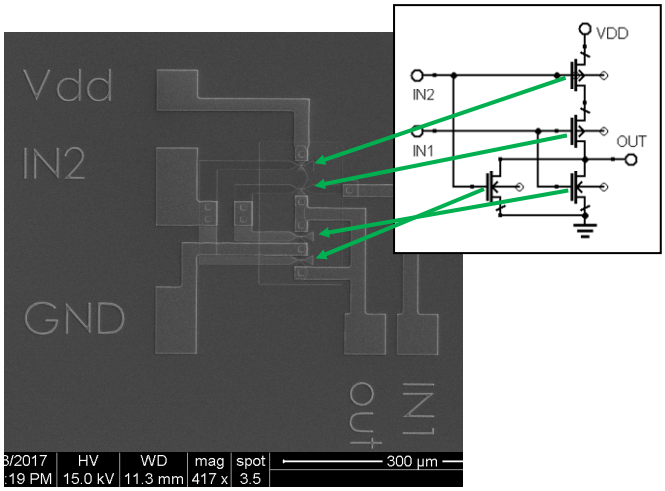


Fig. 3. A SEM image of the NOR gate with single load pVeSFETs.

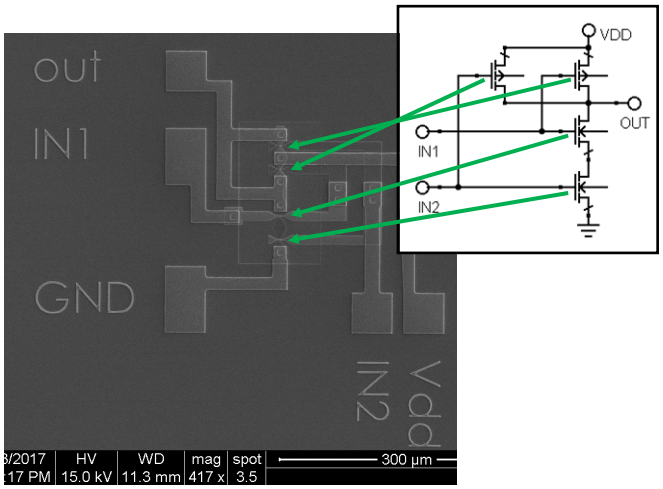


Fig. 4. A SEM image of the NAND gate with single load pVeSFETs.

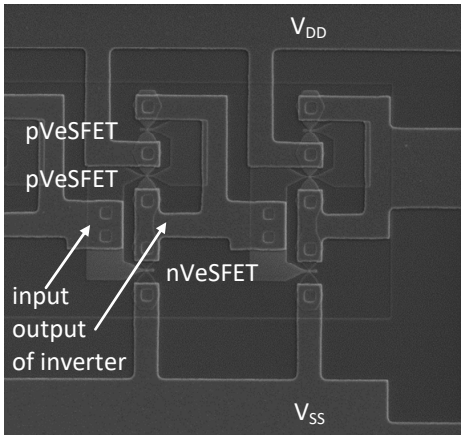


Fig. 5. SEM image of two stages of the CMOS ring oscillator.

A difference between the actual VeSFET architecture and the "ideal design" [1, 2] is clearly visible. Only the slit has a characteristic circular shape, the radius of which is nominally 500 nm. The slit width is nominally 300 nm.

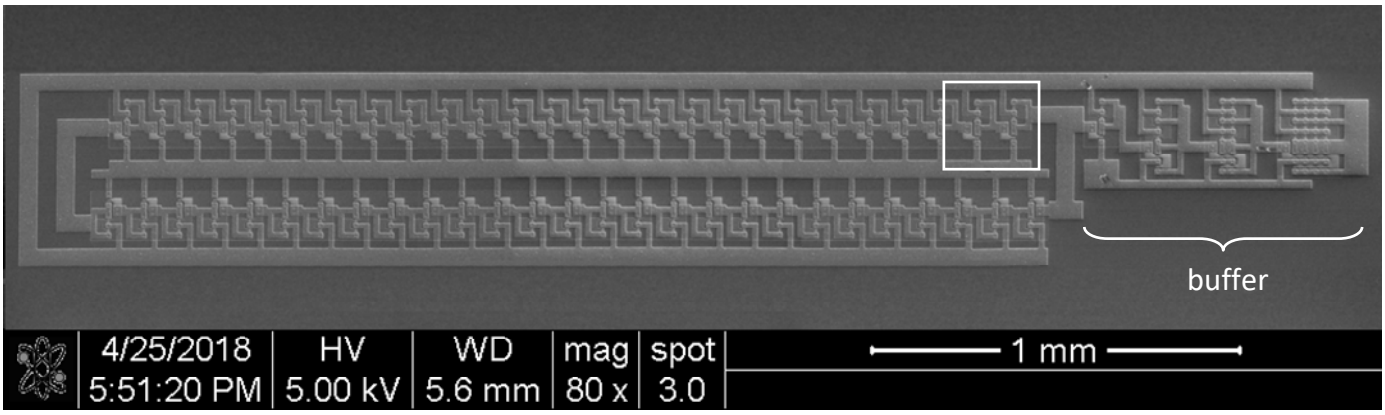


Fig. 6. SEM picture of the 53 stage CMOS ring oscillator manufactured in VeSTIC process; the circuit contains a buffer for probing; marked two stages shown in larger magnification in Fig. 2.

Large areas of polysilicon (at the inverter input, and connecting gates of both p-type devices) and of the metallization are noticeable. It may be expected that they introduce large parasitic capacitances and resistances affecting the RO dynamic operation.

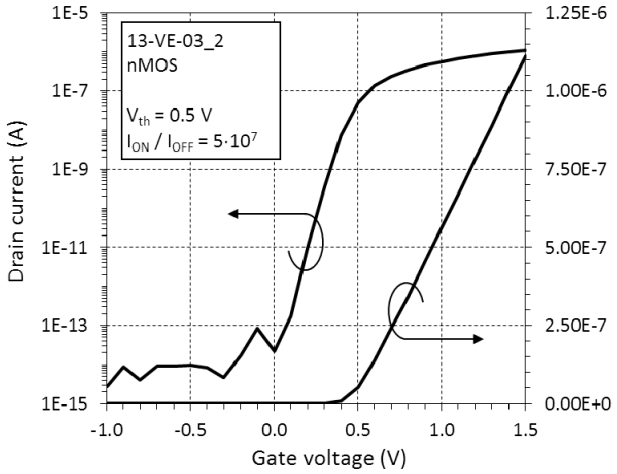
IV. Test Device and Circuit Measurements

Electrical measurements of the devices, logic cells and ring oscillators were made on wafers using the Keithley 4200 semiconductor characterization system equipped with source-measure units (SMUs) for DC measurements and a scope unit Keithley 4200-SCP2 for RO waveforms acquisition. The characterization system was combined with the CASCADE MICROTECH probe station SUMMIT 12000B-AP.

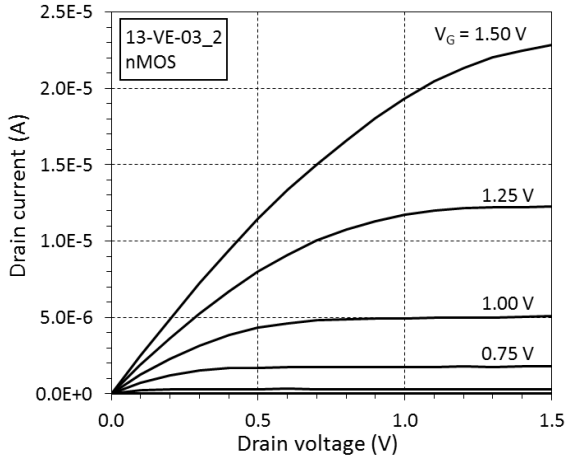
A. DC measurements of the VeSFETs

The test circuit measurements were preceded by extensive DC measurements of the I-V characteristics of the individual VeSFETs. The measurement results proved that the process was developed correctly. However, a large spread of the VeSFET characteristics was noticeable [10]. First of all, it was due to the variability of the photolithography and patterning steps. Proper conditions of these operations imposed by requirements of the VeSTIC process could not be sufficiently provided using the available photolithography equipment. This led to a significant variability of the slit height and width. The slit width variability is of particular importance, because for the correct device opration it must be strictly correlated with the slit doping concentration. Additionally, the plasma etching of the slits iduced a large roughnes of the fin sidewall surfaces. Though reduced (see Section II), this effect led to a non-negligible defect density on the surface of the VeSFET channel. All the factors, mentioned above, were responsible for the experimentally observed spread of the device characteristics.

The DC I-V characteristics of single n- and p-channel VeSFETs are shown in Fig. 7, and Fig. 8. They exhibit a correct transistor current efficiency. The threshold voltages $V_{th,n}\approx 0.5$ V, $V_{th,p}\approx -1.0$ V, though not symmetrical, were acceptable. The VeSFETs demonstrated an excellent subthreshold slope $SS_n\approx 61$ mV/dec, $SS_p\approx 75$ mV/dec, and a high I_{ON}/I_{OFF} ratio, namely $I_{ON}/I_{OFF,n}=5\cdot 10^7$, $I_{ON}/I_{OFF,p}=10^8$. Such promising characteristics of the VeSFETs were predicted earlier by numerical simulations [4, 7].



a)



b)

Fig. 7. Input (a), and output (b) I-V characteristics of the nVeSFET.

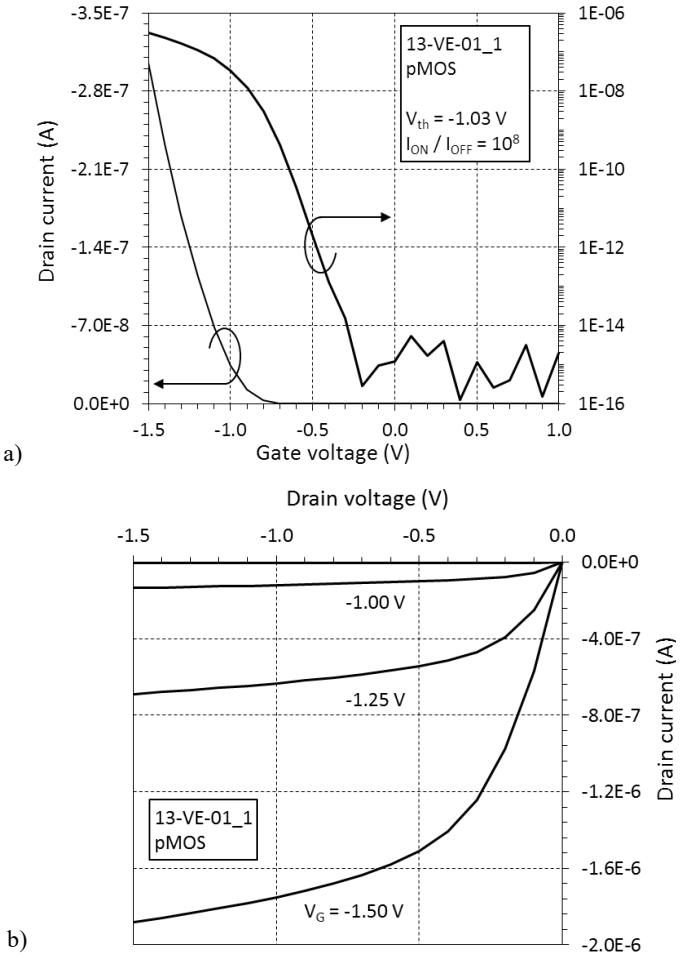


Fig. 8. Input (a), and output (b) I-V characteristics of the pVeSFET.

B. *DC measurements of the logic gates*

The DC measurements of the inverters and logic gates in the VeSTIC test structure have shown their acceptable behavior, although some shortcomings have been also revealed.

The transfer $V_{out}(V_{in})$ and $I_{dd}(V_{in})$ characteristics of the inverter are shown in Fig. 9. In order to partially compensate the threshold voltage unsymmetry between the n- and p-channel VeSFETs, the substrate was biased at -10 V. However, due to a large variability of the transistors, the substrate bias improving characteristics of one device could not necessarily have a positive impact on the characteristics of another device. We suppose, that the device variability could be a reason for the fact, that the $I_{dd}(V_{in})$ characteristics in Fig. 9 demonstrated a relatively large supply current if the pVeSFET was switched-off.

The DC transfer characteristics of the NOR and NAND gates are shown in Fig. 10. The gates correctly responded to the voltage waveforms at the input terminals. However, going into details shown in Fig. 11 and Fig. 12, relatively large current levels were measured not only during the switching, but in the steady-state as well. In the NOR gate, if two gate inputs were at the low level, and the output was at the high level, the bias source V_{DD} provided a steady-state current I_{DD} order of 30 nA. On the other side, if at least one input was at the high level (the output was at the low level) the steady-state current I_{DD} provided by the V_{DD} source was low. Also in this case the partially incorrect behavior of I_{DD} current of the NOR gate can be probably attributed to the large variability of the device characteristics, which was very difficult to be compensated by the substrate bias.

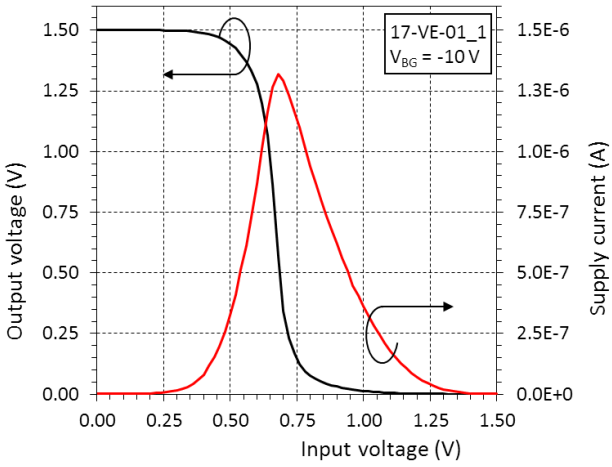


Fig. 9. $V_{out}(V_{in})$ and $I_{dd}(V_{in})$ characteristics of the inverter in VeSTIC process.

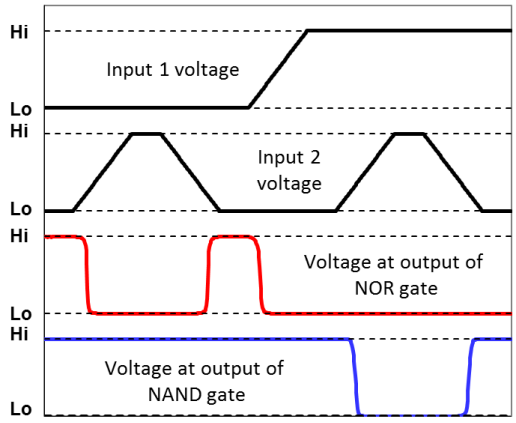


Fig. 10. Output voltage waveforms of the NOR and NAND gates.

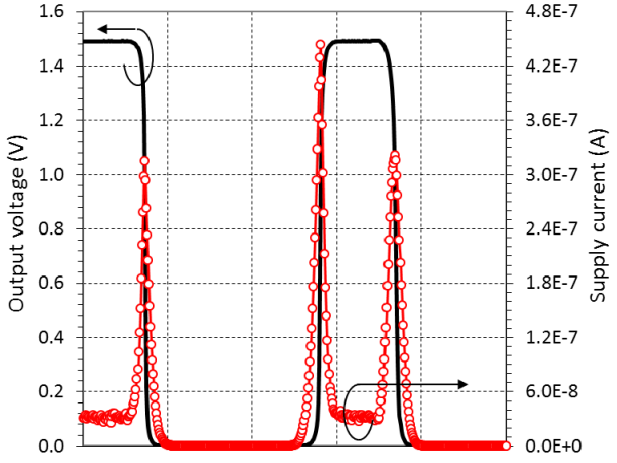


Fig. 11. Output voltage and supply current waveforms of the NOR gate.

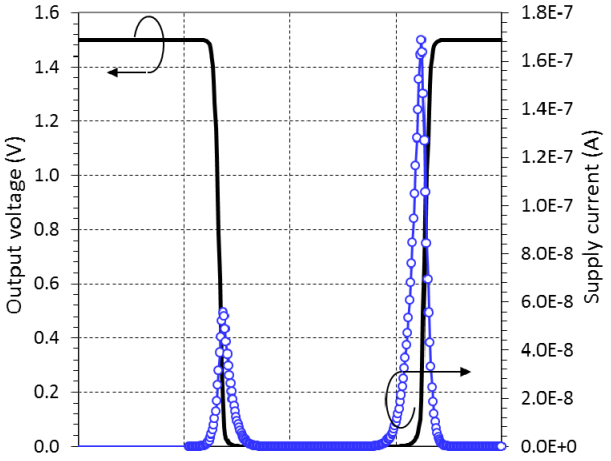


Fig. 12. Output voltage and supply current waveforms of the NAND gate.

C. *Measurements of the ring oscillator*

Electrical measurements of the voltage waveforms in the 53-stage ring oscillator finalized the test device/circuit characterization.

In Fig. 13 two waveforms generated by the RO are shown. As expected, a strong effect of the supply bias on the oscillation frequency is clearly visible. However, the oscillation frequencies were low. Based on (1), where N=53 is the number of stages

$$f_{osc} = 1/[N \cdot (t_r + t_f)] \quad (1)$$

the frequency f_{osc} of 0.8 MHz at V_{DD}=3V corresponds to a sum of the inverter rise and fall times t_r+t_f=23.6 ns, whereas f_{osc}=1.1 MHz at V_{DD}=5V corresponds to t_r+t_f=17.2 ns. It was not a satisfactory result. Moreover it is visible, that the saw-like waveforms did not reach in both cases the levels of V_{SS}=0 V, and V_{DD}. Based on these observation it could be concluded that the inverter/oscillator operation was strongly affected by large paracitic capacitances and/or resistances which together with insufficient current efficiency of the transistors made the time delays too large to form the waveforms of the correct shape. Moreover, it could be stated that the waveforms did not reach the V_{SS} and V_{DD} levels.

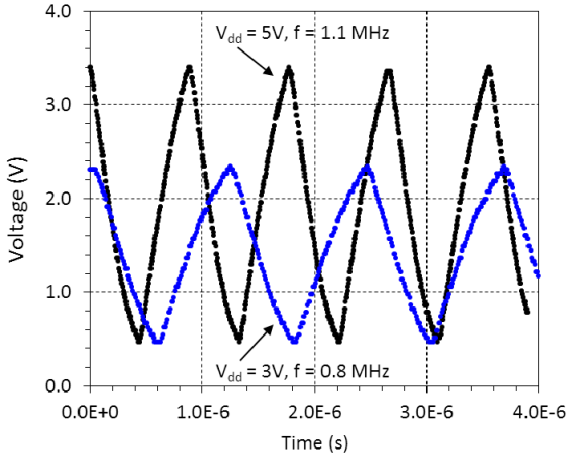


Fig. 13. Waveforms of the ring oscillator measured for two supply voltages

So, the oscillator consumed a large amount of the static power. The effect of the parasitics on the oscillation frequency will be discussed in the next sections.

In Fig. 14 an effect of the substrate bias on the RO operation is illustrated. The most pronounced effect was a shift of the waveforms along the voltage axis. The negative substrate bias increased the pVeSFET channel conductance. In parallel it decreased the conductance of nVeSFETs. This led to the waveform shift shown in Fig. 14. It is also worthwhile to mention, that contrary to V_{DD} voltage, the substrate bias had a negligible effect on the oscillation amplitudes. However, a small but clear effect of the substrate bias on the oscillation frequency was discovered. It is illustrated in a brief form in Fig. 15.

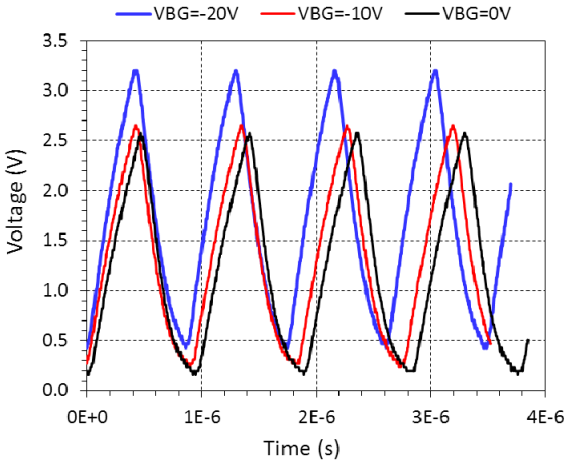


Fig. 14. Waveforms of the ring oscillator measured for different substrate bias

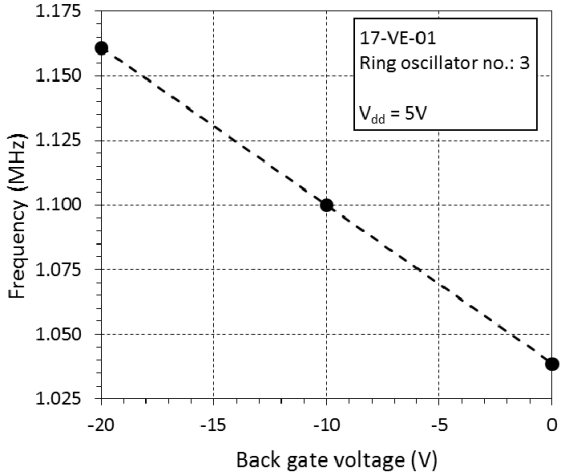


Fig. 15. Effect of back gate voltage on RO frequency.

V. Extraction of Parasitic Elements in the VeSTIC CMOS Inverter

Parasitic elements of the inverter were determined based on the circuit layout, shown in Fig. 5 and illustrated in Fig. 16, where the parasitic elements were assigned to different regions of the inverter. Their characteristic values were estimated based on the corresponding region size and wafer/process data. Brief specifications of these elements along with their values are listed in Table I.

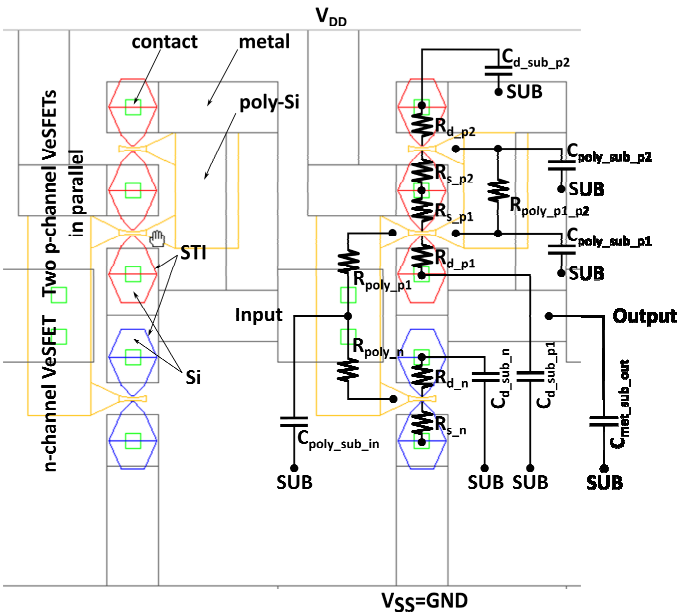


Fig. 16. A layout of the VeSFET-based CMOS inverter used in the ring oscillator design; parasitic passive elements are assigned to different regions of the inverter.

Three groups of large parasitic capacitances are clearly noticeable, i.e. $C_{d\_sub\_x}$, $C_{poly\_sub\_x}$, $C_{met\_sub\_x}$ between the areas of silicon, polysilicon and metallization and wafer substrate. They are of the order of 20 fF, 40 to130 fF, 120 fF accordingly. As compared to them, the capacitances between the VeSFET gates and channels $C_{g\_chan\_x}$, though having a thin gate oxide (7 nm) are at least ten times lower. The capacitances between the VeSFET channels and the substrate are negligible.

There are two types of large parasitic resistances resulting from the inverter layout, namely the serial resistances of the VeSFET source/drain areas, and resistances of the polysilicon lines. The source/drain resistances $R_{s/d\_n/p1/p2}$ are due to the source/drain contacts and to the access regions between the contacts and the channels. The access region thickness is 190 nm, same as in the slits. Based on the earlier work, these resistances are approximately 11 kΩ [14]. The polysilicon resistances, order of 2 to 3 kΩ, are determined by the poly-Si sheet resistance $R_{s,poly}$=220 Ω and the poly-Si line length-to-width ratios, which are of the order of 10, if the line narrowings are taken into account.

TABLE I.
PASSIVE ELEMENTS ASSOCIATED WITH DIFFERENT REGIONS OF THE INVERTER

Element	Unit	Specification	area below 7nm gate oxide on sidewalls of slit (m^2)	area below 100nm gate oxide on top of slit (m^2)	area above 400nm BOX (m^2) or L/W of poly-Si resistors (R_s=220 Ω)	oxide thickness (m) or sheet resistance (Ω)	C (F) or R (Ω)
$C_{poly\_sub\_in}$	F	capacitance: poly-Si at inverter input / substrate			$1.52 \cdot 10^{-9}$	$4.0 \cdot 10^{-7}$	$1.31 \cdot 10^{-13}$
R_{poly_n}	Ω	serial resistance: input / gate of NMOS transistor			8.0	220	$1.76 \cdot 10^{3}$
R_{poly_p1}	Ω	serial resistance: input / gate of PMOS1 transistor			8.0	220	$1.76 \cdot 10^{3}$
$R_{poly\_p1\_p2}$	Ω	serial resistance: PMOS1 gate / PMOS2 gate			13.5	220	$2.97 \cdot 10^{3}$
$C_{poly\_sub\_p1}$	F	capacitance: poly-Si of PMOS1 gate / substrate			$4.66 \cdot 10^{-10}$	$4.0 \cdot 10^{-7}$	$4.02 \cdot 10^{-14}$
$C_{poly\_sub\_p2}$	F	capacitance: poly-Si of PMOS2 gate / substrate			$4.66 \cdot 10^{-10}$	$4.0 \cdot 10^{-7}$	$4.02 \cdot 10^{-14}$
R_{s_n}	Ω	serial resistance of source of NMOS transistor					$1.10 \cdot 10^{4}$
R_{d_n}	Ω	serial resistance of drain of NMOS transistor					$1.10 \cdot 10^{4}$
R_{s_p1}	Ω	serial resistance of source of PMOS1 transistor					$1.10 \cdot 10^{4}$
R_{d_p1}	Ω	serial resistance of drain of PMOS1 transistor					$1.10 \cdot 10^{4}$
R_{s_p2}	Ω	serial resistance of source of PMOS2 transistor					$1.10 \cdot 10^{4}$
R_{d_p2}	Ω	serial resistance of drain of PMOS2 transistor					$1.10 \cdot 10^{4}$
$C_{g\_chan\_n}$	F	capacitance: NMOS gate / channel	$5.97 \cdot 10^{-13}$	$5.15 \cdot 10^{-13}$			$3.12 \cdot 10^{-15}$
$C_{chan\_sub\_n}$	F	capacitance: NMOS channel / substrate			$5.15 \cdot 10^{-13}$	$4.0 \cdot 10^{-7}$	$4.44 \cdot 10^{-17}$
$C_{d\_sub\_n}$	F	capacitance: NMOS drain / substrate			$2.38 \cdot 10^{-10}$	$4.0 \cdot 10^{-7}$	$2.05 \cdot 10^{-14}$
$C_{g\_chan\_p1}$	F	capacitance: PMOS1 gate / channel	$5.97 \cdot 10^{-13}$	$5.15 \cdot 10^{-13}$			$3.12 \cdot 10^{-15}$
$C_{chan\_sub\_p1}$	F	capacitance: PMOS1 channel / substrate			$5.15 \cdot 10^{-13}$	$4.0 \cdot 10^{-7}$	$4.44 \cdot 10^{-17}$
$C_{d\_sub\_p1}$	F	capacitance: PMOS1 drain / substrate			$2.38 \cdot 10^{-10}$	$4.0 \cdot 10^{-7}$	$2.05 \cdot 10^{-14}$
$C_{g\_chan\_p2}$	F	capacitance: PMOS2 gate / channel	$5.97 \cdot 10^{-13}$	$5.15 \cdot 10^{-13}$			$3.12 \cdot 10^{-15}$
$C_{chan\_sub\_p2}$	F	capacitance: PMOS2 channel / substrate			$5.15 \cdot 10^{-13}$	$4.0 \cdot 10^{-7}$	$4.44 \cdot 10^{-17}$
$C_{d\_sub\_p2}$	F	capacitance: PMOS2 drain / substrate			$2.38 \cdot 10^{-10}$	$4.0 \cdot 10^{-7}$	$2.05 \cdot 10^{-14}$
$C_{met\_sub\_out}$	F	capacitance: metal at the output / substrate			$2.64 \cdot 10^{-9}$	$7.8 \cdot 10^{-7}$	$1.17 \cdot 10^{-13}$

VI. Estimation of Propagation Times and Oscillation Frequency of the Ring Oscillator

The inverter propagation times can be estimated based on an equivalent circuit representing the inverter, and taking account its dominant parasitic elements. This circuit, drawn based on the diagram in Fig. 16, is shown in Fig. 17.

The rise and fall propagation times may be determined using the Elmore method presented in [16]. The rise time corresponds to the state where the p-type transistors are open and the capacitances at the inverter output are charged by the voltage source V_{DD}. It is illustrated by the equivalent circuit in Fig. 18. Analogously, the fall time corresponds to the state where the n-type transistor is open and the capacitances at the inverter output are discharged. It is illustrated by the equivalent circuit in Fig. 19. $R_{chan\_n/p1/p2}$ denote the resistances of the n-, pVeSFET open channels. C_{load} is the total capacitance originating from the next stage input. These parameters are defined by (2), (3).

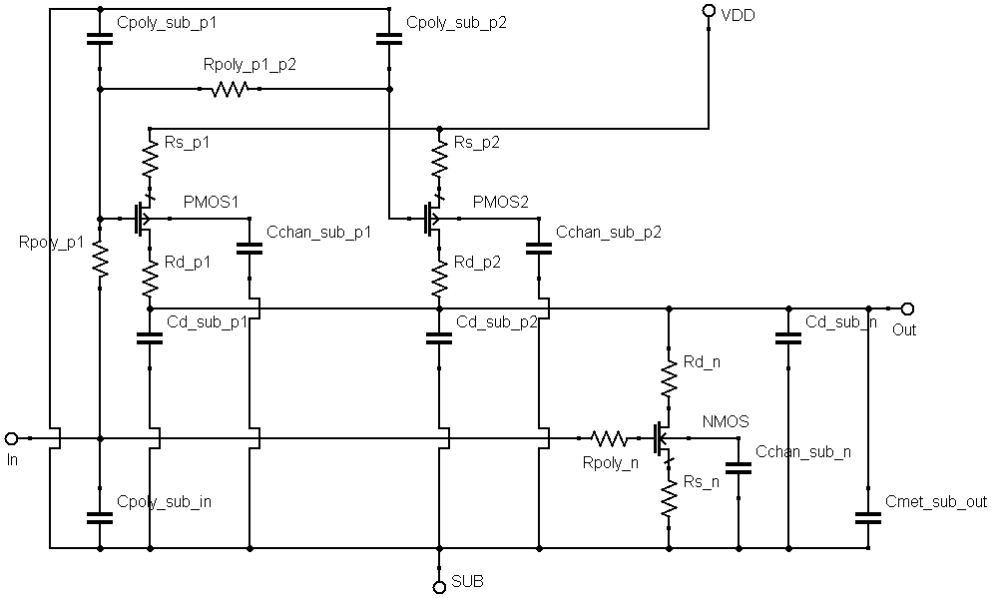


Fig. 17. An equivalent circuit of a single VeSTIC inverter including the parasitic passive devices; the gate-channel capacitances in the transistors are not directly marked.

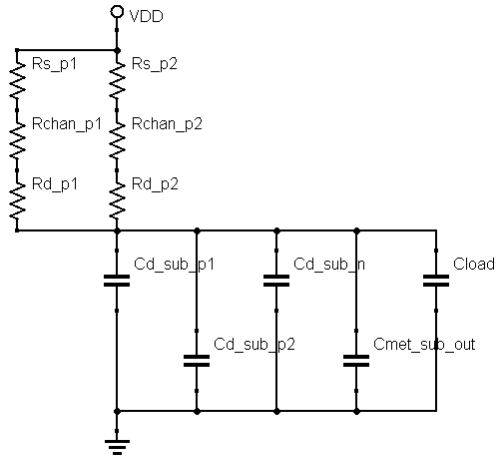


Fig. 18. An equivalent circuit of a single VeSTIC inverter for estimation of rise time t_r.

The formula (2) results from a very simple model of the MOSFET I-V characteristics in the saturation range. The n- and pVeSFET transconductance factors β_n, β_p were determined based on the I-V measurements: $\beta_n \approx 4 \cdot 10^{-5}$ A/V^2, $\beta_p \approx 3 \cdot 10^{-5}$ A/V^2.

$$R_{chan\_n/p1/p2} \approx V_{DD}/I_{D\_n/p1/p2} \approx 1/(\beta_{n/p}/2 \cdot V_{DD}) \quad (2)$$

$$C_{load} = C_{poly\_sub\_in} + C_{poly\_sub\_p1} + C_{poly\_sub\_p2} + C_{g\_chan\_p1} + C_{g\_chan\_p2} + C_{g\_chan\_n} \quad (3)$$

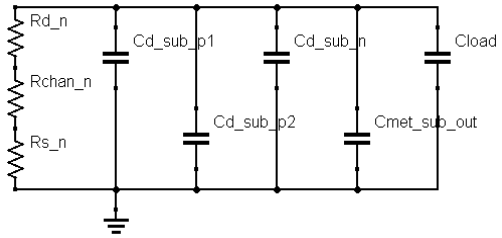


Fig. 19. An equivalent circuit of a single VeSTIC inverter for estimation of fall time t_f.

With these parameters, and following [15] the t_r, t_f times may be calculated as RC-constants of networks in Figs. 18, 19 accordingly. The estimated inverter propagation times and calculated and measured oscillation frequencies are listed in Table II.

TABLE II.
RING OSCILLATOR PARAMETERS

Parameter	Unit	V_{DD}=3 V	V_{DD}=5 V
R_{chanp1}	Ω	$2.222 \cdot 10^4$	$1.333 \cdot 10^4$
R_{chanp2}	Ω	$2.222 \cdot 10^4$	$1.333 \cdot 10^4$
t_r	s	$8.823 \cdot 10^{-9}$	$7.050 \cdot 10^{-9}$
R_{chann}	Ω	$1.667 \cdot 10^4$	$1.000E \cdot 10^4$
t_f	s	$1.543 \cdot 10^{-8}$	$1.277 \cdot 10^{-8}$
f_{osc}	Hz	$7.780 \cdot 10^5$	$9.520 \cdot 10^5$
$f_{osc\ meas}$ (Fig.5)	Hz	$8.000 \cdot 10^5$	$1.100 \cdot 10^6$

It may be stated, that the the estimated oscillation frequencies remain in a relatively close agreement with the measured values. However, the V_{DD} voltage effect on these parameters is in theory weaker than as measured. However, it should be noted that the calculations shown above are based on a very simple model. We have not taken into account the parasitic elements associated with the buffer block. Also the method of the VeSFET channel resistance calculation is very simple as compared e.g. with [4].

VII. Characteristics of the Ring Oscillator in "Ideal" VeSTIC Process

In this section the RO oscillation frequency will be estimated for a hypothetical process, which allows for manufacturing of the VeSFETs shown in Fig. 2 in the work [4]. It will be assumed, that the characteristic radius of the process is 500 nm (same as in Fig. 1). The Si film and gate oxide thicknesses, Si doping, poly-Si sheet resistance are also the same as in the real process. The poly-Si and metallization lines do not overlap. A layout of the inverters used for estimation of the parasitic elements is shown in Fig. 20.

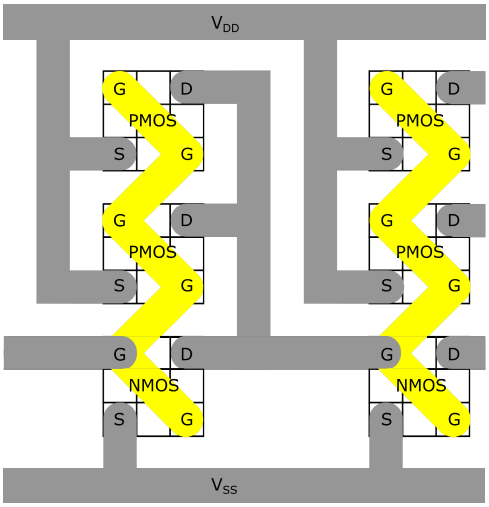


Fig. 20. A layout of the RO stages approximating the quasi-ideal design.

The updated parasitic elements, which affect the t_r, t_f, f_{osc} parameters according to Figs. 18, 19, are listed in Table III. The calculated RO parameters are listed in Table IV. It is clearly visible, that thanks to radical decrease of the size of the RO elements and the connecting lines, the oscillation frequency has been improved by a factor of 60.

VIII. Summary

A study on a characterization of the logic integrated circuits designed and fabricated in ITE using the CMOS VeSTIC process has been presented. This technology, which has been described in detail, is more challenging than any other ones developed in ITE. It allows for manufacturing integrated circuits witt the lowest critical dimension. The VeSFETs, operating correctly, with the channel widths even below 50 nm have been manufactured. However the measurement results have revealed several shortcomings of this technology in its current state. Firstly, due to the non-ideal

TABLE III.
Ring oscillator parameters in the quasi-ideal case

Element	area above 400nm BOX (m^2) or L/W of poly-Si resistors (R_s=220 Ω)	C (F) or R (Ω)
$C_{poly\_sub\_in}$	$5.0 \cdot 10^{-12}$	$4.31 \cdot 10^{-16}$
$C_{poly\_sub\_p1}$	$3.0 \cdot 10^{-12}$	$2.59 \cdot 10^{-16}$
$C_{poly\_sub\_p2}$	$3.0 \cdot 10^{-12}$	$2.59 \cdot 10^{-16}$
R_{s_n}, R_{d_n}, R_{s_p1}, R_{d_p1}, R_{s_p2}, R_{d_p2}		$1.75 \cdot 10^{3}$
$C_{g\_chan\_n}$		$3.12 \cdot 10^{-15}$
$C_{chan\_sub\_n}$	$5.15 \cdot 10^{-13}$	$4.44 \cdot 10^{-17}$
$C_{d\_sub\_n}$	$1.0 \cdot 10^{-12}$	$8.63 \cdot 10^{-17}$
$C_{g\_chan\_p1}$		$3.12 \cdot 10^{-15}$
$C_{chan\_sub\_p1}$	$5.15 \cdot 10^{-13}$	$4.44 \cdot 10^{-17}$
$C_{d\_sub\_p1}$	$1.0 \cdot 10^{-12}$	$8.63 \cdot 10^{-17}$
$C_{g\_chan\_p2}$		$3.12 \cdot 10^{-15}$
$C_{chan\_sub\_p2}$	$5.15 \cdot 10^{-13}$	$4.44 \cdot 10^{-17}$
$C_{d\_sub\_p2}$	$1.0 \cdot 10^{-12}$	$8.63 \cdot 10^{-17}$
$C_{met\_sub\_out}$	$1.5 \cdot 10^{-11}$	$6.64 \cdot 10^{-16}$

TABLE IV.
Ring oscillator parameters in the quasi-ideal case

Parameter	Unit	V_{DD}=3 V	V_{DD}=5 V
t_r	s	$1.446 \cdot 10^{-10}$	$9.462 \cdot 10^{-11}$
t_f	s	$2.267 \cdot 10^{-10}$	$1.518 \cdot 10^{-10}$
f_{osc}	Hz	$5.082 \cdot 10^{7}$	$7.658 \cdot 10^{7}$

VeSFET channel control, the logic gates exhibit a significant DC power consumption, which is demonstrated by the not full transition of the gate outputs between the low and high levels. Secondly, the process suffers from significant variability of the device characteristics. This variability is mainly due to the inacurracies in the photolithography and patterning steps, resulting from the limitations of the process equipment (e.g. too poor resolution of the photoresist development). This has led to the too large variability of the channel size in the VeSFETs. While the slit width must be strictly correlated with the slit doping for the proper operation of the VeSFETs, the variability is of particular importance for the VeSTIC circuits design and yield. Finally, due to the large parasitic capacitances and resistances introduced implicitly by the logic cell design, the circuits under consideration exhibit a slow transient operation. Therefore the oscillation frequency of the RO is very low. These large parasitic capacitances have been introduced by the conservative design methodology, which has been used in order to ensure a reliable DC operation of the circuits.

In order analyze the ring oscillator measurement characteristics, a simple model of the inverter fabricated in ITE has been proposed. The model takes into account the

parasitic capacitances and resistances induced by the device topography. A satisfactory agreement between the experimental and calculated data has been obtained. The analysis has shown, that wide polysilicon and metallization lines are responsible for the inverter/ring oscillator behaviour in the time domain.

REFERENCES

[1] W. Maly, “Integrated Circuit, Device, System, and Method of Fabrication”, U.S Patent 2009/0321830, Dec. 31, 2009

[2] W. Maly and A. Pfitzner, “Complementary vertical transistors”, Carnegie Mellon Univ., Pittsburgh, PA, CSSI Tech. Rep. 08-02, Jan. 2008

[3] W. Maly *et al.*, “Twin gate, vertical slit FET (VeSFET) for highly periodic layout and 3D integration”, Proc. 18th Int. Conf. MIXDES, 2011, pp. 145–150

[4] A. Pfitzner, “Vertical-Slit Field-Effect Transistor (VeSFET) - design space exploration and DC model”, Proc. 18th Int. Conf. MIXDES, 2011, pp. 151–156

[5] A. Pfitzner, M. Staniewski, M. Strzyga, "DC Characteristics of Junction Vertical Slit Field-Effect Transistor (JVeSFET)”, Proc. 16th Int. Conf. MIXDES, 2009, pp. 420-422

[6] P. Mierzwiński, W. Kuźmicz, K. Domański, D. Tomaszewski, G. Gluszko, "Bipolar transistor in VESTIC technology: prototype", Proc.SPIE 10175, Electron Technology Conference 2016

[7] P-L. Yang, T. B. Hook, P. J. Oldiges and B. B. Doris, “Vertical Slit FET at 7-nm Node and Beyond”, IEEE Trans. Electron Devices, 2016, Vol.63, No. 8, pp. 3327 – 3334, 2016.

[8] Z. Chen, A. Kamath, N. Singh, N. Shen, X. Li, G.-Q. Lo, D.-L. Kwong, D. Kasprowicz, A. Pfitzner, W. Maly, "N-channel Junction-less Vertical Slit Field-Effect Transistor (VeSFET): Fabrication-based Feasibility Assessment", Proc. 2012 Int. Conf. Solid-State and Integrated Circuit (ICSIC 2012)

[9] D. Tomaszewski, K. Domański, G. Głuszko, A. Sierakowski and D. Szmigiel, "MOSFETs in the VeSTIC process - fabrication and characterization," 2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), 2017, pp. 71-74

[10] G. Głuszko, D. Tomaszewski and K. Domański, "Electrical characterization of different types of transistors fabricated in VeSTIC process", Proc. 24th Int. Conf. MIXDES, 2017, pp. 132-136

[11] M. Pastre, F. Krummenacher, L. Barbut., J.-M. Sallese, M. Kayal, "Towards Circuit design Using VeSFETs", Proc. 18th Int. Conf. MIXDES, 2011, pp. 139-144

[12] A. Kamath, Z. Chen, N. Shen, N. Singh, G. Q. Lo, D.-L. Kwong, D. Kasprowicz, A. Pfitzner, W. Maly, "Realizing AND and OR Functions With Single Vertical-Slit Field-Effect Transistor", IEEE Electron Device Let., Vol. 33, No. 2, pp. 152-154, 2012

[13] P.-L. Yang, M. Marek-Sadowska, W. Maly, "Performance assessment of VeSFET-based SRAM", Proc. 2015 IEEE Int. Conf. Electron Devices and Solid-State Circuits (EDSSC), pp. 79-82

[14] D. Tomaszewski, K. Domański, G. Głuszko, A. Sierakowski, D. Szmigiel, "An Effect of Device Topology in VeSTIC Process on Logic Circuit Operation - A Study Based on Ring Oscillator Operation Analysis", Proc. 25th Int. Conf. MIXDES, 2018, pp. 51-56

[15] D. Tomaszewski, G. Głuszko, J. Malesińska, K. Domański, M. Zaborowski, K. Kucharski, D. Szmigiel, A. Sierakowski, "A Simple Method for Characterization of MOSFET Serial Resistance Asymmetry", Proc. 28th IEEE Int. Conf. on Microelectronic Test Structures, Phoenix, 23-26.03.2015, pp. 116-121

[16] N. H. E. Weste, D. Harris, "CMOS VLSI Design - A Circuits and Systems Perspective", 3rd Ed., Pearson Education, Inc., 2005