Low Ripple Current Mode Charge Pumps with Parasitics Precharge

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***Abstract*— In this paper a novel current mode charge pump architecture is shown and discussed. The presented DC-DC voltage converter uses extremely low filtering capacitance while still maintaining a low ripple amplitude of the output voltage. The proposed architecture is silicon proven in CMOS 130 nm technology. The power efficiency and layout area trade-offs of the proposed architecture are considered also.**

***Index Terms*—charge pump; low ripple; voltage doubler**

I. Introduction

CHARGE pumps are fully integrated on-chip DC-DC voltage converters. The main role of charge pumps is providing an internal voltage that is higher than the system supply voltage. Such circuits are applied in semiconductor memories [1], [2], Micro-Electro-Mechanical-Systems (MEMS) [3], Radio Frequency Identification Cards (RFID) [4], sensors [5] etc.

There are several challenges in charge pump design: sufficient level of output voltage, power efficiency, reliability, silicon area occupied on integrated circuit, low ripple amplitude of the output voltage. The last requirement has been studied more carefully in this paper. Selected strategies of low ripple charge pump design have been presented first. This provides background for introducing the new current mode architecture [6]. In the end the key advantages and disadvantages of the new architecture are considered.

Ripples of the output voltage are detrimental to the operation of the circuit using the pump and should be minimized. For example in [7] a MEMS capacitor in an RF filter is tuned with the voltage generated by a charge pump. A noisy tuning voltage generated by the pump would interfere with the main system frequency.

II. Ripples in Conventional Charge Pumps

Modern conventional charge pumps use an array of capacitors (usually called "pumping" or "flying" capacitors) to store energy. The stored energy is transferred to the load and output "filtering" capacitor by periodically reconfigured switches (see Fig. 1). The output voltage of the pump is higher than the supply voltage level because pumping capacitors (C_{FLY}) operate as a voltage level shifter. At least two phases of operation are required (the flying capacitor charge regeneration phase and the charge transfer phase). The presented conventional charge pump configuration is often called a Charge Transfer Switch pump (CTS pump). In a conventional CTS pump the charge is transferred to the filtering capacitor and load only within selected moments. During the remaining time no charge is transferred to the load (Fig. 1). For this reason using a filtering capacitor is mandatory. In order to keep the ripple amplitude of the output voltage at a sufficiently low level, the filtering capacitance needs to be large enough. The chip area occupied by the filtering capacitor may be considerable therefore the total chip area occupied by the pump becomes large as well. Chip manufacturers are continuously looking for cost reduction by reducing the chip area. The semiconductor industry is interested in charge pumps with reduced filtering capacitor area and low ripple amplitude of the output voltage at the same time.

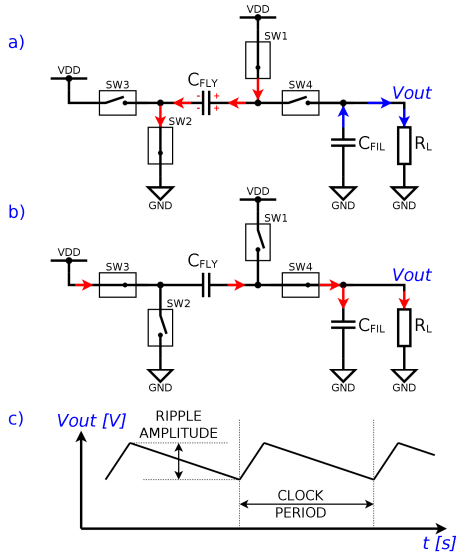

Fig. 1. Basic architecture of a conventional CTS charge pump and its operation: a) charge regeneration phase, b) charge transfer phase, c) output voltage plot.

Several techniques for ripple reduction are known. They are briefly introduced here to highlight the current state of the art. The following techniques belong to this group:

- increasing filtering capacitor size and operating frequency,
- interleaved scheme.

The listed techniques have serious drawbacks. In particular increasing the filtering capacitor size generates a high manufacturing cost (chip area is being increased). Increasing the operating frequency of the pump reduces power efficiency

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(because of parasitic elements). The last technique, the interleaved scheme [7], [8], [9], is of great practical importance and is used in the majority of modern DRAM and NVRAM memories charge pump systems. In the interleaved scheme there are several instances of fully operational charge pumps connected in parallel. The pumps are operated with clocks shifted in phase. A more complex clock path leads to increased power dissipation. The area of the circuit is also affected.

III. Conventional Current Mode Charge Pump Architecture

Ripples in the output voltage of the pump are due to discontinuous flow of the charge from the pump to the filtering capacitor and load. In order to reduce the ripples, the period of time during which the charge is transferred to the load, should be increased and the time when charge is not transferred should be decreased. The simplest technique to achieve this goal is to introduce series resistance in the pump output switch [10]. With the increased series resistance of the switch the charge from the charge pump will flow less rapidly to the filtering capacitor and the charge flow from the pump will be prolonged. Simultaneously, some power is lost in the series resistance of the switch. However, with this simple technique it is possible to achieve even a few percent ripple reduction sacrificing less than one percent of power efficiency [11].

In order to reduce the ripple amplitude as much as possible, the pump should deliver constant current rather than a quantum of charge to the load. This idea has been implemented in the current mode pump [3], [12], [13], [14]. Fig. 2 presents the basic current mode pump voltage doubler architecture and its operation.

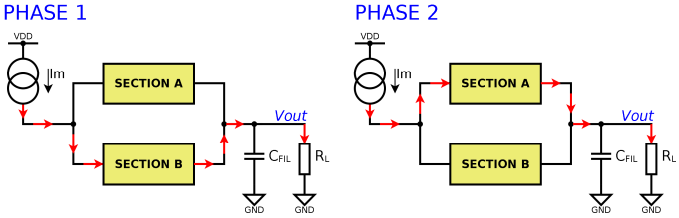

Fig. 2. Operation of a conventional current mode charge pump.

The presented voltage doubler uses a constant current source generating current *Im*. Current *Im* is flowing through a selected section (either section A or B) to the load (R_L) connected in parallel with the filtering capacitor (C_{FIL}). Each of the presented sections contains a flying capacitor and switches. The flying capacitors are initially charged. When the current *Im* is flowing through the selected section, the charged flying capacitor operates as a voltage level shifter. Consequently the voltage delivered by the pump to the load is higher than the system supply voltage (*VDD*). The flying capacitors are being discharged during one phase of pump operation (when current flows through them to the load) and need to be recharged during the second phase. In order to continuously deliver constant current from the charge pump to the load two sections of the pump are needed. If the current flows through section B (phase 1) the flying capacitor in the section A is being recharged. In the second phase of operation the current path is switched to section A, while the flying capacitor in section B is being recharged. The drawback of using current mode architecture is a slight loss of power efficiency (in comparison with the conventional CTS pump). The extra power is dissipated in the current source (the *Im* current multiplied by the voltage drop across the current source). An advantage of this architecture is significant reduction of the ripple in the pump output voltage. That is because constant current *Im* flowing from the pump to the resistive load R_L should not produce any ripple. This assumption is difficult to meet in practice. A more detailed look at the architecture of this pump reveals several issues related to switching of the current path.

IV. Influence of the Parasitic Capacitance

Fig. 3 presents the architecture of the current mode voltage doubler charge pump. The parasitic elements related to the flying capacitor C_{FLYB} were presented as additional capacitors CP1 and CP2. Similar parasitic elements exist for the flying capacitor C_{FLYA}, but were not illustrated here. The parasitic capacitance plays an important role in the pump operation. In Fig. 3 the first phase of operation is presented in detail. In this phase the switches SW3A and SW4A are conducting. The current *Im* flows through the flying capacitor C_{FLYA} to the load R_L connected in parallel with the filtering capacitor C_{FIL}. The flying capacitor C_{FLYA} was initially charged and operates as a voltage level shifter now. It enables the pump output voltage *Vout* (which is 1.5 V in this example) to be higher than the supply voltage *VDD* (which is 1.2 V). The current *Im* is tuned so as to keep the pump output voltage constant. The *Im* tuning circuitry is not presented here. Assuming the load R_L is resistive, the current *Im* is constant. During the first phase of operation (Fig. 3) the switches SW1B and SW2B are also conducting. The second flying capacitor C_{FLYB} is being recharged. Flying capacitors are usually fabricated as MOS type capacitors (using gate oxide leads to high unit capacitance and saves chip area). Unfortunately, this type of capacitor has significant parasitic capacitances, modeled here as CP1 and CP2 elements. When the flying capacitor C_{FLYB} is being recharged the parasitic capacitances CP1 and CP2 are also charged and discharged to the potentials marked in Fig. 3. In particular, CP1 is being discharged and CP2 is being charged to supply voltage *VDD* (1.2 V).

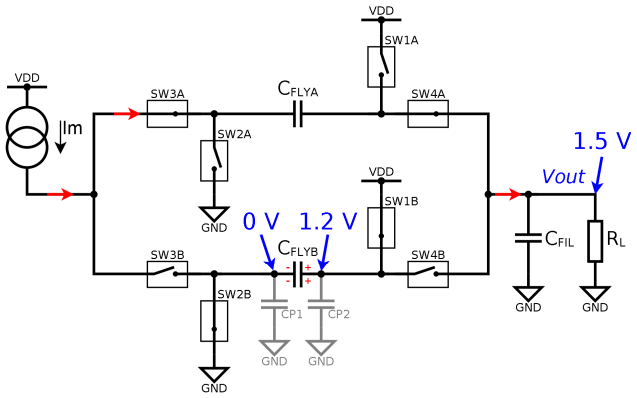

Fig. 3. Current mode charge pump voltage doubler. First phase of operation.

In Fig. 4 the beginning of the second phase of pump operation is presented. The switches are being reconfigured and SW1A, SW2A, SW3B, SW4B are conducting now. The first pair of switches (SW1A, SW2A) charges the flying capacitor C_{FLYA}. Conducting switches SW3B and SW4B provide a current path from *Im* current source through the flying capacitor C_{FLYB} to the load R_L. In the second phase of pump operation the *Im* current was supposed to flow through the C_{FLYB} flying capacitor to the load, but it is not happening immediately after switch reconfiguration because of the influence of the parasitic capacitances (CP1, CP2). As seen in Fig. 4 the parasitic element CP1 is discharged at that moment. As a consequence the current *Im* flows to the discharged parasitic capacitance CP1. In addition the CP2 potential (1.2 V) is lower than the pump output voltage (1.5 V). This causes a reverse current flow from the filtering capacitor C_{FIL} to the parasitic capacitance CP2. The reverse current flow and the fact that the *Im* current does not flow to the load increases the pump output voltage ripple amplitude. After a while (within the same phase of pump operation) the parasitic capacitances will be charged to the desired potentials and the current *Im* will flow to the load as expected.

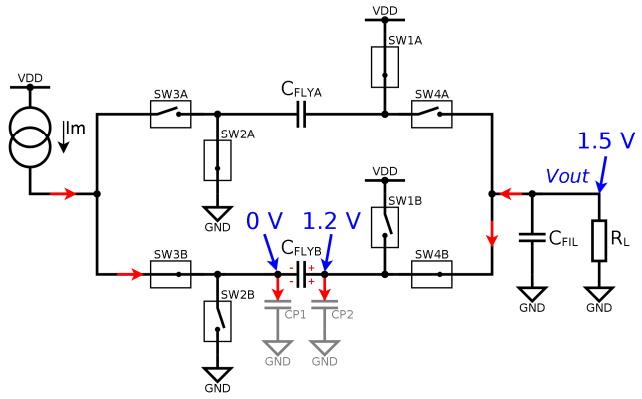

Fig. 4. Beginning of the second phase of operation of the current mode charge pump.

The conclusion is that the parasitic capacitance plays an important role in ripple creation. Does the parasitic capacitance play an important role in all types of pumps or is it just an issue specific to the current mode charge pump? Definitely this problem exists in all the pumps, but is usually underestimated. It is very important for two reasons: the ripple amplitude increase and the power efficiency drop.

In conventional charge pump architecture a really large (overdesigned in a way) filtering capacitance must be used. The large filtering capacitance reduces ripples that originate from the discontinuous charge transfer from pump to load. The ripples originating from the parasitic capacitances are filtered as well. That is why the influence of the parasitic capacitance is not analyzed separately in conventional pumps. But in the current mode pump the ripple amplitude is lower and the filtering capacitance is reduced. The parasitic capacitance starts to play a dominant role in ripple characteristics.

The second issue present in all types of charge pumps is power efficiency drop caused by parasitic capacitance. Parasitic capacitance related to the pumping capacitor is charged and discharged in every clock cycle and the power required for this process is lost. The parasitic capacitances related to the flying capacitors are relatively large (up to 10% in CMOS technologies [15]). Therefore increasing the operating frequency in order to reduce the ripple amplitude of the pump output voltage may lead to serious power consumption increase. Other techniques (such as current mode pump, which operates with low switching frequency) may yield better results.

V. Precharging Parasitic Capacitance

In [16] a novel parasitic precharge mechanism was first introduced. The parasitic precharge concept is presented in Fig. 5. The main idea is that two additional current sources supplying currents *Ipa* and *Ipb* have been added. The additional current sources are being activated during additional phases of operation. During the remaining time these current sources are inactive and do not provide any current. In Fig. 5 the additional phase of operation is illustrated. During this phase the main current *Im* flows through the flying capacitor C_{FLYA} (similarly to the first phase of operation presented earlier in Fig. 3). The flying capacitor C_{FLYB} was first charged through switches SW1B, SW2B and is fully charged now. During the additional phase of operation the switches SW1B and SW2B are in the high impedance state. The current source providing current Ipb is being activated now. The *Ipb* current charges up the parasitic capacitances CP1 and CP2. When the parasitic capacitances CP1 and CP2 are charged up to proper levels (which would be about 0.3 V and 1.5 V in this particular example) the additional current source is deactivated and the current *Ipb* does not flow. At this moment the pump is ready for switching the main current *Im* path (not illustrated here). The benefit of precharging the parasitic capacitances is that the main current flow *Im* is not disturbed and the reverse current flow from the filtering capacitor C_{FLY} to the parasitic capacitance CP2 is also avoided. The presented third phase of operation and the mechanism of precharging parasitic capacitances make the main current flow immune to the parasitics influence. The ripple amplitude of the pump output voltage is greatly reduced.

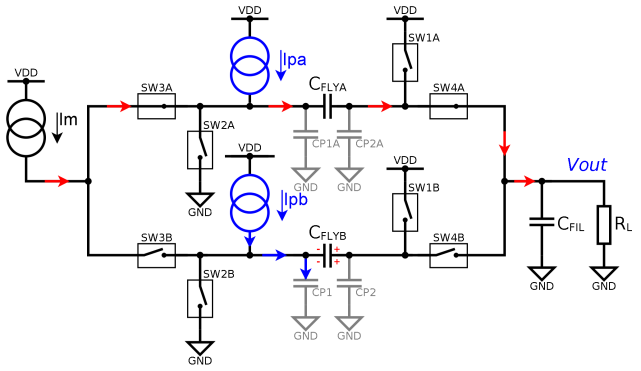

Fig. 5. Proposed parasitic precharge phase of operation.

In the proposed architecture the amount of the additional charge (delivered by currents *Ipa* and *Ipb*) is of key importance. If this amount is not enough, the ripple cancellation effect will not be full. On the other hand, if the amount of the additional charge is too large ripples of opposite

sign will appear. It was proposed to tune the amount of the additional charge by tuning the length of time during which the additional current sources are active. The control mechanism and the control loop implementation are explained in details in [16] and [17].

In Fig. 5 the voltage doubler architecture is used to explain how the parasitic precharge mechanism reduces the ripples of the current mode pump output voltage. In [18] it was demonstrated that a similar technique could be used for multistage charge pumps. The paper presents simulation data on low ripple pump implementing the proposed parasitic precharging method. The pump is supplied from 1.2 V and delivers 6.0 V output voltages. In subsequent sections silicon proven voltage doubler prototype will be presented in details.

VI. Current Mode Voltage Doubler Prototype

A current mode voltage doubler was designed and fabricated in UMC CMOS 130 nm technology process. The main goal of designing the prototype was to compare the conventional current mode architecture with the proposed architecture featuring the parasitic precharge mechanism. In particular the influence of the parasitics and the operation of the proposed control loop were examined. The prototype was designed according to the circuitry in Fig 5. The following functional blocks are also required but were not illustrated in Fig. 5: the parasitic precharge control loop, an oscillator and clock generation path, reference currents generator, on-chip test and mode select circuitry (for reference please see [16], [17] and [18]). The prototype is a standalone design, providing charge pump testing ability without the need for external clock or references. Before presenting the measurement results it is important to understand test challenges for charge pumps. During the prototype design it was extremely important to measure its characteristics on a CASCADE measuring station using conventional probes. There are several issues related to the measurements of the characteristics of charge pump ripple. The most important one is that test equipment may influence the results. In particular the capacitance of the filtering capacitor (C_{FIL}) attached to the pump output may be as low as several picofarads. The capacitance of a conventional probe with one-meter triaxial (triax) cable attached is more than 100 picofarads. Connecting the probe directly to the pump output means that the capacitance of the coaxial cable would play the role of a filtering capacitor. The measured output voltage ripples would become smaller because of the influence of the measurement equipment as opposed to normal operation conditions (without measurement equipment). Considering this fact on-chip test equipment was designed in accordance with Fig. 6.

The charge pump supplies a constant current to an on-chip load resistor R_L connected in parallel with the filtering capacitor C_{FIL}. The pump output voltage can be measured directly on VT2 pad. However, during the standard measurement procedure this pad is left unconnected to avoid the influence of the measurement equipment. The pump output is connected to the gate of a NMOS transistor MN operating as an amplifier in the source follower configuration. In this

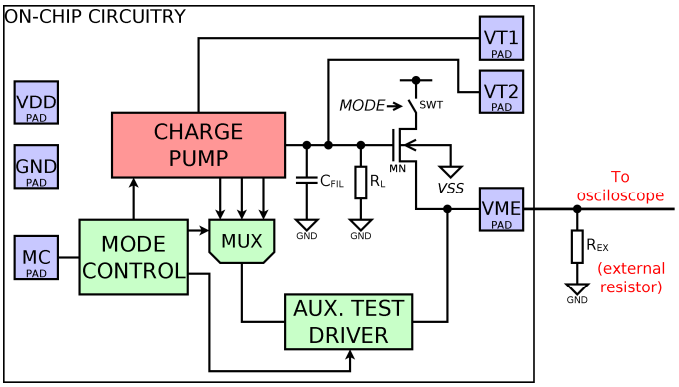

Fig. 6. On-chip measurement and test architecture. Pad description: VDD, GND – power supply and ground, respectively, MC – Mode Control, VT1, VT2 – test voltages (not used in the standard measurement procedure), VME – main voltage for standard measurement procedure.

configuration any influence on the pump output voltage is minimized. The transistor source is connected to VME external pad. The load for the NMOS transistor is an external resistor R_{EX} on which voltage drop is measured. The circuitry parameters are adjusted so that the ripple amplitude measured on the external resistor R_{EX} is two times smaller than the actual pump output voltage ripples on the load resistor R_L.

The general characteristics of the IC prototype are presented in Table I. The layout of the designed voltage doubler is shown in Fig. 7 [19]. The micrograph of the manufactured chip is presented in Fig. 8. The voltage doubler architecture was chosen for its simplicity. The pump supply voltage *VDD* is 1.2 V and the output voltage *Vout* is 1.5 V, so the prototype voltage conversion ratio is relatively low. However, it should be noted that the proposed ripple reduction techniques may be also implemented in pumps delivering higher output voltages. In particular low ripple hybrid pump solution was presented in [19]. The most important parameter of the IC prototype is the filtering capacitance (1.6 pF), which is only a fraction of the pumping capacitance (there are two flying capacitors 15.2 pF each). Such low filtering capacitance was never reported before. It should be understood that it is a key parameter distinguishing the proposed pump architecture from other known architectures.

TABLE I.
General Characteristics of the Prototype

Parameter	*Value*
Technology	CMOS UMC 130 nm
Supply voltage	VDD = 1.2 V
Pump output voltage	VOUT = 1.5 V
On-chip load RL	RL = 190 KΩ
External load REX	REX = 1.2 KΩ
Operating frequency	2.27 MHz
Total area occupied on chip	118000 µm2 (314 µm x 376 µm)
Total area occupied on chip excluding pads area	56000 µm2
Flying capacitance	CFLY = 15.2 pF
Filter capacitance	CFIL = 1.6 pF

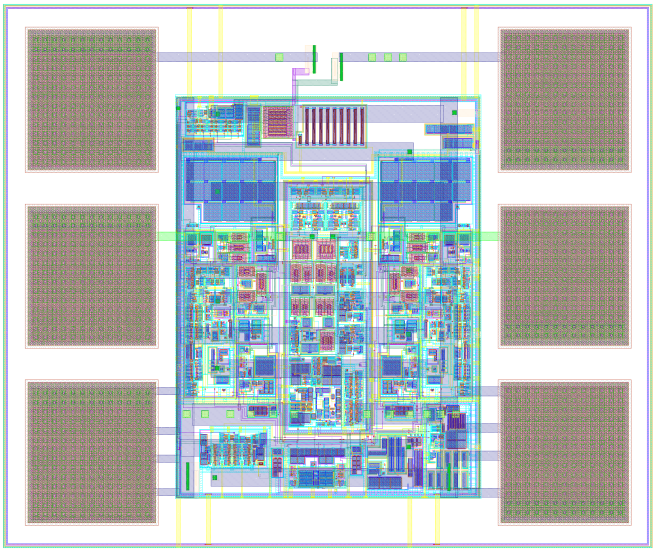

Fig. 7. The layout of designed voltage doubler.

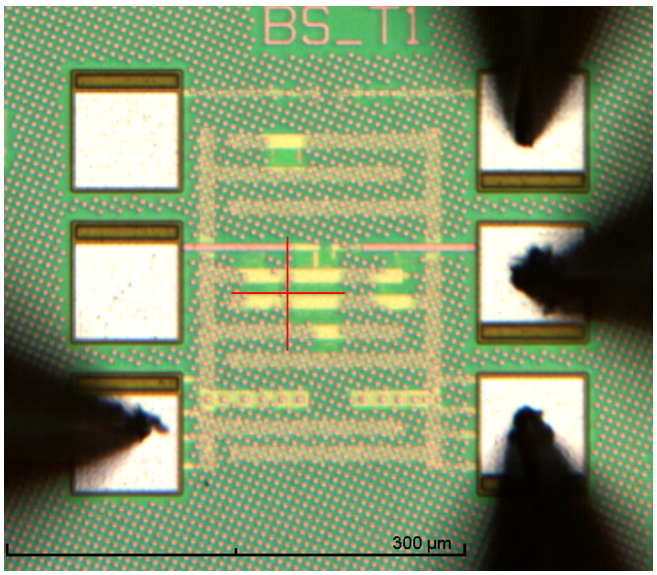

Fig. 8. Micrograph of the prototype voltage doubler. Four probes attached.

The prototype has two main modes of operation and several test modes. The first mode of operation is called "reference mode". In the reference mode the prototype operates as a conventional current mode charge pump (the additional current sources for parasitic capacitance precharge are disabled). No parasitic precharge mechanism is present and therefore the parasitic influence on the ripple amplitude of the output voltage can be observed. The second mode of operation is called "basic mode". In basic mode the proposed parasitic precharge mechanism is activated and ripple cancellation can be observed. The only difference between the two modes is the activation of the additional current sources; no other architectural changes are made. Comparing pump operation in both modes yields precise information about the influence of the parasitic capacitance. Apart from those two modes there are also several test modes for internal voltage monitoring and circuitry diagnostics (the test modes will not be described in detail here). In Fig. 9 the IC prototype measurements are presented. The plot presents the voltage measured across the external resistor R_{EX} for two modes of operation (first for reference mode and then the basic mode). The time scale and the voltage scale are the same (although the time scale is discontinuous). It is silicon-proven that the proposed parasitic precharging mechanism reduces the ripple amplitude of the pump output voltage significantly.

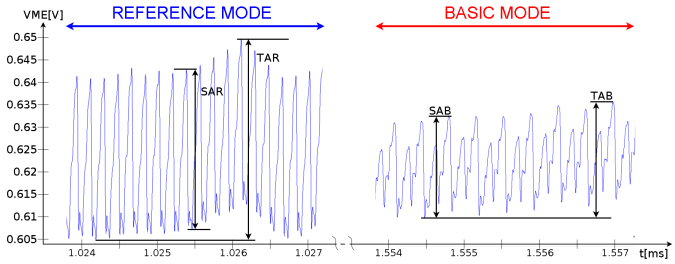

Fig. 9. Measured voltage across the external resistor.

The plot reveals how certain ripple amplitude characteristics were defined. The first letter in each acronym stands for S-Short term ripple or T-Total ripple amplitude. The last letter indicates the mode of operation (R-Reference mode or B-Basic mode). For example TAR acronym stands for Total (long term) ripple Amplitude for charge pump operating in the Reference mode. The main goal of the proposed parasitic precharge mechanism is to reduce short-term ripples. The plot in Fig. 9 is a single measurement of the prototype chip while the data averaged over five prototype structures is presented in Table II. Please note that the actual ripple amplitude of the pump output voltage is two times higher than the presented ripple characteristics of the external resistor voltage.

TABLE II.
EXTERNAL RESISTOR VOLTAGE RIPPLE AMPLITUDES.
SUPPLY VOLTAGE VDD = 1.185 V

	Ripple amplitude parameter					
	TAB [mV]	***TAR [mV]***	***Reduction (Total ripple)***	***SAB [mV]***	***SAR [mV]***	***Reduction (Short - term ripple)***
Measurements	39	58	32.75%	25.2	39.7	36.47%

The averaged ripple reduction in the basic mode of operation is 36% for short term ripple amplitude (SAR and SAB parameters). This means that the voltage ripple amplitude at the external resistor decreases from 39.7 mV to 25.5 mV on average. When the external resistor ripple amplitude is about 25 mV it means that the pump output voltage ripple amplitude is 50 mV. The prototype was originally designed to obtain the ripple amplitudes of the pump output voltage at 15 mV level in the basic mode in the worst case (7.5 mV ripple would be observed at the external resistor). There are several reasons for the difference between the initial design specifications and measurement results. The supply model used for the simulations was inaccurate. In particular the IC prototype was measured using a probe station without bonding and it was not possible to avoid long connections between the measured structure and the test equipment. The impedance of a one-meter triax coaxial cable between supply and the prototype plays an important role. Simulations with corrected supply models match measurement

results. Increasing on-chip decoupling would improve ripple characteristics, but the chip was not re-designed and silicon proved so far. Although the prototype characteristics were worse than expected, the proposed parasitic precharge mechanism was experimentally tested and gave satisfactory results of 36% ripple reduction with extremely low pump filtering capacitance of 1.6 pF only.

VII. Layout Area Trade-offs

One of the main advantages of using the proposed architecture is the ability to reduce the filtering capacitance. The area usage of the individual functional blocks of the prototype is presented in Table III. The filtering capacitor area is only a fraction of the pumping capacitor area. This is an important observation that has never been reported so far. It demonstrates that the pump architecture is truly low ripple and requires only a very small filtering capacitor in comparison to its pumping capacitors. Usually the filtering capacitor is much larger than the pumping capacitors [17].

TABLE III.
Prototype layout area

	IC Prototype
Total pump area (pads excluded)	56000 μm^2
Test and mode select	2200 μm^2
Reference currents generator	2400 μm^2
Filtering capacitor area	300 μm^2
Pumping capacitors total area	3800 μm^2
Parasitic precharge mechanism components	20000 μm^2
Remaining components, routing, guard ring, etc.	27300 μm^2

In UMC CMOS 130 nm technology the total cost of implementing the parasitic precharge circuitry is 20000 μm^2. An obvious question appears. When does it make sense to use the proposed architecture in order to save layout area (since the parasitic precharge circuitry requires extra area) and when it is better to use the conventional CTS pump? A general assumption can be made that the area required by the pump is a linear function of the pump's maximum output current. It is because the conventional charge pump area depends mostly on the size of the pumping and filtering capacitors. With current increase the charge pump needs both pumping and filtering capacitors larger. The pumping capacitance is increased because more charge needs to be delivered. The filtering capacitor increase is dictated by the need to maintain the same ripple amplitude while currents increase.

In the conventional CTS architecture the filtering capacitor is larger than the pumping capacitors. When the maximum output current of a CTS pump is increased the increased size of the filtering capacitor plays the dominant role. It should be noted, therefore, that the proposed architecture uses a relatively small filtering capacitor but requires additional area dedicated for the parasitic precharge circuitry. Therefore for small pump output currents the conventional CTS architecture is better (it is better to increase the filtering capacitor size instead of designing a complicated control loop for parasitic precharging). For larger output currents the proposed architecture will be better.

It was estimated that for the UMC CMOS 130 nm process the proposed architecture demonstrates layout area reduction advantage over conventional CTS architecture for output current greater than 21 μA (additional assumptions: same operating frequency, output voltage and ripple amplitude level). Taking into account significantly more complicated circuitry the recommendation for using the proposed architecture for area reduction would be for pumps supplying at least tens of microamperes of output current.

VIII. Power Efficiency Trade-offs

There are several reasons for which power is lost in charge pumps. Similarly to any CMOS circuit power dissipation increases with increasing frequency. Other important phenomena are the series resistance of the switches and possible difficulties with controlling the "on" and "off" states of the high voltage switches (which may result in undesired current flows). All these issues are observed in both conventional Charge Transfer Switch (CTS) and current mode pumps.

In current mode charge pumps there are two more issues resulting in power efficiency degradation. The main current source requires a certain voltage drop to operate properly (usually hundreds of millivolts). Therefore, it dissipates power. Moreover, the proposed parasitic precharge control loop consumes power for its proper operation (the loop consists of analog elements requiring biasing and supply).

The post-layout simulation data concerning the power consumption of the IC prototype is presented in Table IV. Only the pump and the on-chip load are considered (no data on test environment power consumption). In the prototype 11.8 μW of power is delivered to the load, while the total power consumption of the pump is 69.1 μW. The prototype power efficiency is 17.1%. However, it should be noted that there is a significant contribution of the supporting circuitry in power consumption (for example the oscillator consumes substantial power regardless of the pump load conditions).

TABLE IV.
Prototype power consumption. Simulation

	Prototype	***Increased output current***
Total power consumption (Ptotal) including:	69.1 μW	129.2 μW
- circuitry related to charge transfer (main current source, switches)	29.0 μW	86.8 μW
- supporting circuitry (oscillator, current reference, voltage regulator)	29.2 μW	31.2 μW
- proposed parasitic precharge control loop	10.2 μW	11.16 μW
Total power delivered to load (Pload)	11.8 μW	47.2 μW
Power Efficiency	17.1 %	36.5 %

In order to fully understand the power consumption characteristics of the proposed architecture another simulation was performed (the results are presented in the last column of

Table IV). In the second simulation the pump output current was increased four times. In order to achieve such increase the load resistance was decreased and the pumping and filtering capacitances were increased proportionally. All the remaining pump circuitry and parameters such as operating frequency were kept unchanged. In this case the power efficiency is 36.5%. The data in the table reveals that the "supporting circuitry" power dissipation is almost constant, while the power dissipation of the circuitry related to the charge transfer depends on the pump output current. If the total power consumption of the pump were approximated as a linear function of the power delivered from pump to load, the formula that would satisfy the data presented in Table IV would be:

$$Ptotal = 55.6\ \mu W + 1.7 * Pload. \quad (1)$$

Increasing the power delivered from pump to load by 1 µW requires additional 1.7 µW of power consumed by the pump from supply. If the constant power consumption of 55.6 µW were neglected (which would be justified for relatively high powers delivered to load), the theoretical maximum power efficiency may be calculated. In the IC prototype it reaches 1 divided by 1.7, which is 58.8%.

It was claimed that the power efficiency of current mode pumps is usually lower than that of CTS pumps. However, this conclusion may be shortsighted. The current mode pumps have the advantage of operating at low frequency. The prototype operates at 2.27 MHz (2.68 MHz measured). On the contrary, the conventional CTS type charge pumps operate at higher frequencies in order to keep the output voltage ripples low. Increased operating frequency results in increased power dissipation. It would be interesting to directly compare the power efficiency of both pump types. In order to do that two more simulations were performed. In the first simulation a conventional CTS pump according to the architecture presented in Fig. 1 was simulated. The main idea was to keep the operating conditions similar to those of the prototype. The flying capacitor and load were exactly the same as in the current mode prototype. The filtering capacitor had to be increased to a capacitance that equals four times the capacitance of the flying capacitor, which is a typical value in CTS pumps. The CTS pump would not operate properly with the filtering capacitance as low as it was demonstrated in the proposed architecture. In order to accurately estimate power efficiency post-layout extraction was performed for key elements. Any supporting circuitry power consumption was neglected. The simulation results are gathered in Table V.

TABLE V.
CTS PUMP POWER CONSUMPTION. SIMULATION

Operating frequency	*Output voltage*	*Ripple Amplitude*	*Power efficiency*
4 MHz	2.194 V	32 mV	80.7%
10 MHz	2.272 V	20 mV	60.7%

The CTS pump power efficiency drops rapidly with operating frequency increase. Attempting to keep low ripple in CTS pump only by operating frequency increase is ineffective.

IX. CONCLUSIONS

The properties of the proposed current mode pump with parasitic precharge mechanism determine its particular applications. The proposed architecture requires a significantly lower filtering capacitance in comparison to conventional architectures, which leads to chip area reduction. There is one more advantage related to the reduced size of the filtering capacitor. The pump start-up time is greatly reduced because it is easy to charge-up a small filtering capacitor. In particular the prototype activation takes approx. 2.5 µs (the output voltage ramps up from 0.7 V to 1.5 V, power up sequence time not included). The start-up time of a conventional CTS pump is longer. For example in [20] a comparable start up time of 2.9 µs is presented, but operating frequency is 60 MHz (low power efficiency).

There are also disadvantages of the proposed current mode pump not mentioned so far. Low filtering capacitance makes the pump sensitive to load current consumption spikes. In the whole analysis it was assumed that the load is resistive. If the load changes its current consumption dynamically, it will not be compensated by the pump filtering capacitance. In that case the pump output voltage will vary according to the immediate current consumption of the load. Another disadvantage is high sensitivity to the supply noise. If the supply is noisy, the noise will reach the pump output. The conventional CTS charge pump is more immune to the supply noise. The supply noise as well as the noise introduced by pump operation is filtered in a large filtering capacitance. In the proposed architecture the supply noise should be carefully considered in the total noise characteristics of the pump output voltage.

Finally, taking all the pros and cons into account, the potential applications of the proposed architecture can be pointed out. The features of the application that would make it benefit the most from the proposed architecture are:

- low power consumption,
- long standby and short activation time,
- resistive load supplied from the pump.

According to the above requirements a grid of smart sensors is a reasonable example. The sensors would analyze an environmental parameter and the pump would supply the sensing element (for example MEMS) only during short periods of time. Other applications are possible, too. The authors hope that this paper will help understand better the properties of the proposed current mode pump architecture.

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