A 2.3-dB NF CMOS Low Voltage LNA Optimized for Medical Applications at 600MHz

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***Abstract*—In this paper it is presented a balun LNA, with voltage gain control that combines a common-gate and common-source stage, in which transistors biased in triode region replace the resistive loads. This last approach in conjunction with a dynamic threshold reduction technique allows a low supply voltage operation. Furthermore, a significant chip area reduction can be exploited by adopting an inductor-less configuration. Simulations results with a 130 nm CMOS technology show that the gain is up to 19.3 dB and the NF is below 2.3 dB. The total dissipation is 4 mW, leading to an FOM of 2.26 for 0.6 V supply.**

***Index Terms*—DTMOS; balun; low voltage; low power**

I. INTRODUCTION

THE present project for wireless communications includes Industrial, Scientific, and Medical (ISM) and wireless Medical Telemetry Service (WMTS) application [1]. These require low power, low voltage transceivers, which can be fully integrated in a single chip [2, 3], to reduce the area and the cost. A fundamental block in this kind of systems is the Low Noise Amplifier (LNA), which is analyzed in this work.

In this paper, the main goal is to design a low area and low cost LNA, capable to operate at 0.6 V supply voltage with good gain (G) and low noise figure (NF) which can be used in a fall detection microsystem for elder and disable.

Equations for G and NF are presented, which can be used to optimize the circuit performance. Circuit prototypes in 130nm standard CMOS technology at 1.2 V to 0.6 V have been designed and simulated to demonstrate the proposed technique. The circuit prototype at 0.6 V has a gain of 17 dB and NF below 2.3 dB, dissipating only 4 mW, leading to a FOM of 2.26 mW^{-1} is which a high value.

In section II it is described the Low Voltage and Wideband Techniques for LNA. In section III it is presented the proposed circuit to increase gain and reduce NF. In section IV it is presented the simulations results. Finally in section V it is described the conclusions.

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II. LOW VOLTAGE AND WIDEBAND TECHNIQUES FOR A LNA

A. DTMOS technique

The Dynamic Threshold voltage MOS (DTMOS) technique was firstly introduced in 1994, [8], with the objective to better adapt the transistor operation to a lower power supply. The DTMOS technique is mostly used in digital applications in which the gate and the body of the MOSFET are tied together, as shown in Fig 1. In this case, the threshold voltage V_{Th} is higher at $V_{GS}=0$ but reduces when the device turns on, thus facilitating the inversion layer formation near the interface between the oxide and the bulk substrate.

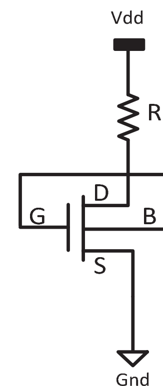

Figure 1. Dynamic threshold MOS (DTMOS).

The threshold voltage of the device in DTMOS configuration is given by

$$V_{Th} = V_{TO} - \gamma * \left(\sqrt{\phi_0} - \sqrt{\phi_0 - V_{BS}}\right) = $$
$$= V_{TO} - \gamma * \left(\sqrt{\phi_0} - \sqrt{\phi_0 - V_{GS}}\right) \quad (1)$$

where, V_{T0} is the value of V_{Th} for $V_{GS}=0$, γ is the body-effect coefficient for a given technology, $\phi_0=2\ \phi_F + \Delta\phi$ (ϕ_F is the Fermi-potential and $\Delta\phi$ is given by $6kT/q \approx 150$ mV at room temperature). Equation (1) clearly shows that the increase of the gate voltage decreases the threshold voltage (V_{Th}), which can be used to improve the level of inversion under low voltage power supply conditions. Not only an higher current can be achieved but also an improvement in its transconductance, g_m , which is given by

$$g_m = \mu C'_{ox} \frac{W}{L} (V_{GS} - V_{Th}) \quad (2)$$

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in saturation (C'_{ox} is the oxide gate capacitance per unit area, W and L are the transistor dimensions and μ is the charge mobility). In addition, the bulk related transconductance, g_{mb}, also contributes to improve the overall device gain.

Figure 2 shows an example of the V_{Th} variation with respect to the bulk source V_{BS} voltage for a 130 nm MOS device.

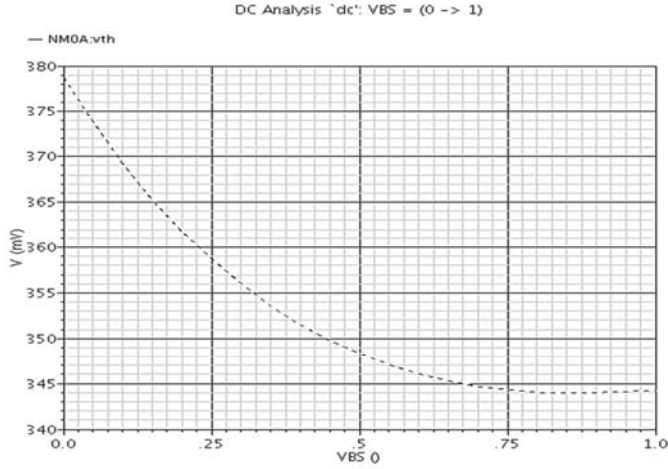

Figure 2. Variation of V_{th} with respect to V_{BS}.

B. Wideband configuration for the I/V load at LNA output

In a traditional LNA, the typical I/V conversion implemented at the output mode is usually based on a LC tank, which contributes for a narrowband frequency response. However, a simple resistor, widening the frequency response of the amplifier, can obtain this I/V operation. One of the problems associated with this approach, under low voltage supply constraints, is the DC voltage drop at the resistor, which can be incompatible with the available total voltage headroom. To overcome this issue, a transistor in triode region can replace the passive resistor, as shown in Fig. 3, since it can reach a similar incremental small signal resistance but with a smaller quiescent DC value for V_{DS}. For example, knowing that the transistor drain current is given by

$$I_D = \mu C'_{ox}\frac{W}{L}\left[(V_{GS}-V_{Th})V_{DS}-\frac{1}{2}{V_{DS}}^2\right] \quad (3)$$

in triode region, a value of 1 mA can be achieved with a V_{DS} as low as 150 mV, considering an 130 nm NMOS device with V_{Th}= 0.38 V, $\mu C'_{ox}W/L$ = 5.25 mAV^{-2} and biased with V_{GS} of 0.6 V. The corresponding small signal resistance r_{ds}, at this quiescent point is approximately 370 Ω. If a passive resistor of this value is used instead, the new DC drop voltage increase significantly to 0.37 V, which can be a major concern for low voltage operation.

An additional advantage of using transistors in triode is the gain tuning capability that can be implemented by connecting a controlling voltage the bulk or the gate, as shown in Fig. 3. On the major drawback of this approach is the distortion introduced the device operating in triode. However, not only the signal amplitudes for the LNA are expected to be small, but also the adoption of a differential structure contributes effectively to reduce the even order distortion effects.

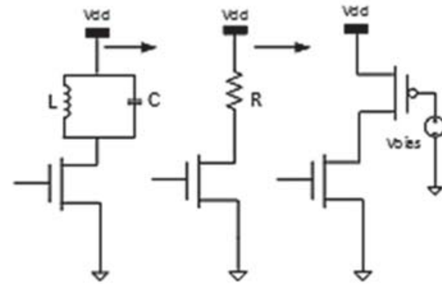

Figure 3. Transistor in triode region with gain tuning.

C. Combined CG and CS used as a Wideband Cancellation Technique

Widening the band of the LNA tends to increase significantly the total input referred noise, since the narrowband filtering has been removed. A possible solution is the balun LNA shown in Fig. 4, [4], in which the thermal noise of M_1 is cancelled out. In fact, the noise produced by M_1 appears in phase at the two output terminals, while the amplified signals that appear at these terminals are in opposition. Therefore, the gain is doubled and the noise is cancelled. It can be shown, [4], that the distortion introduced by M_1 is also reduced (but not totally cancelled).

The differential voltage gain of the LNA is obtained from the gain of a common-gate (CG) stage plus the gain of the common-source (CS) stage:

$$A_v = g_{m1}Rd1 + g_{m2}Rd2\ . \quad (4)$$

As shown in Fig. 4, the gain of the two stages should be equal for balanced balun operation and for noise cancellation. The maximum gain is limited by the value of the resistors since the input matching sets g_{m1}.

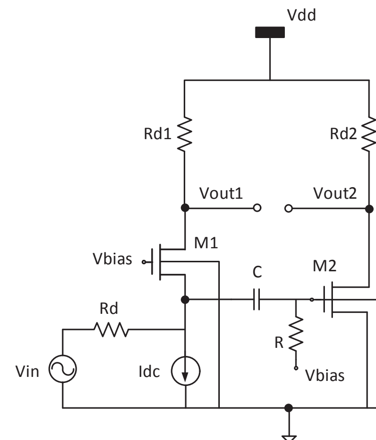

Figure 4. Balun LNA with noise cancellation [4].

III. Proposed LNA with Noise Cancelation and DTMOS Devices

Since g_{m1} is determined by the 50 Ω input matching requirement, higher resistance values are needed to achieve a reasonable gain for the LNA. However, this will difficult the circuit (shown in Fig. 4) operation at low voltage supply due to the large DC voltage drop imposed by those resistors. To overcome the LNA operation problems at 0.6 V, transistors

in triode region can be used to replace the load passive resistors. Additionally, DTMOS configuration is applied in transistors M_1, M_2, M_3, M_4 as it can be seen in Fig. 5.

In the proposed LNA shown in Fig. 5, DTMOS is used to boost the gain, especially when this circuit operates at supply voltage as low as 0.6 V. The buffer was used to make the conversion from differential to single ended.

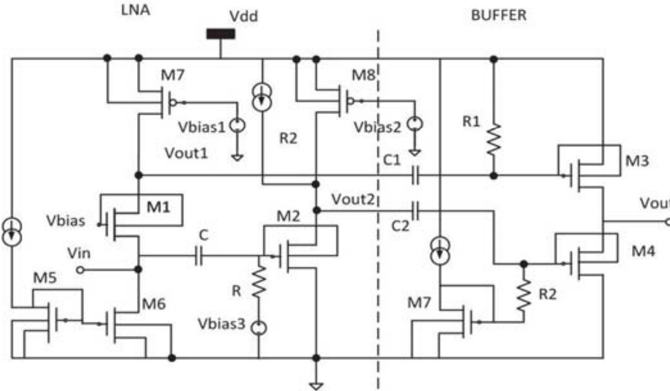

Figure 5. Proposed LNA.

The gain of the proposed LNA as active load is given by:

$$A_v = g_{m1}(r_{d1}//r_{07}) + g_{m1}(r_{d2}//r_{08})\,. \quad (5)$$

The low frequency input impedance is given by:

$$Z_{in} = \frac{1}{g_{m1}+g_{m1b}}\quad . \quad (6)$$

From [4, 9] if it is assumed that $g_{m1} = g_{m2} = g_m$ the noise factor is expressed by:

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S cox f^{\alpha f}}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2}\right) + \frac{\gamma}{2R_{Sgm}} + \frac{1}{R_S ropgm^2}\,. \quad (7)$$

where k is Boltzman's constant, C'_{ox} is the oxide gate capacitance per unit area, W_i and L_i are the transistor dimensions , T is the absolute temperature, γ is the excess noise factor, k_f and α_f are intrinsic process parameters, which depend on the size of the transistors [5, 6] .

IV. Design and Simulation Results

Two circuits were designed and optimized for a 130nm CMOS Standard technology considering 1.2 V and 0.6 V V_{DD}.

The proposed circuit was projected for biomedical applications [1] in situations that require low power and low data rate and to cover the corresponding bands in 450 MHz and 900 MHz and WMTS band in 600 MHz, for which this circuit was optimized.

In the LNA prototype with 1.2 V supply voltage, the transistors have W_1=288 um, W_2=576 µm, W_3=W_4=144 µm, W_7=76.8 µm, W_8=108 µm. For maximum speed, all transistors have the minimum channel length (120 nm) except M_7 which has 240 nm.

For the LNA prototype with 0.6 V supply, the transistors have W_1=288 µm, W_2=576 µm, W_3=W_4=144 µm, W_7=76.8 µm, W_8=64.8 µm. For maximum speed, all transistors have the minimum channel length (120 nm) except M_7 which has 240 nm.

All simulations were performed with Spectre RF software using BSIM3v3 models for a 130 nm CMOS technology. Triple-well option was chosen for the NMOS devices connected in a DTMOS configuration.

TABLE I
Circuit simulations for 1.2 V supply voltage

	BW (GHz)	Av (dB)	NF (dB)	IIP2 (dBm)	IIP3 (dBm)	PDC (mW)	FOM (mW^{-1})
Balun LNA	0.4-0.9	10.5	<3.3	15.3	-3.9	9.5	0.32
Proposed LNA	0.4-0.9	19.3	<2.3	-12.2	-11.2	11.8	1.15

It is seen in Table I that with this configuration a gain boosting of 9 dB is obtained and NF is reduced in 1 dB approximately, and thus corresponding to a better FOM. On the other hand the IIP2 and IIP3 are worsen.

For comparison the following figure merit is used [7]:

$$FOM[mW^{-1}] = \frac{Gain}{(NF-1)P_{DC}[mW]}\,. \quad (8)$$

The noise simulations shown in Fig. 6 and Fig. 7 indicates a slightly degradation of the NF level when the circuit operates at 0.6 V.

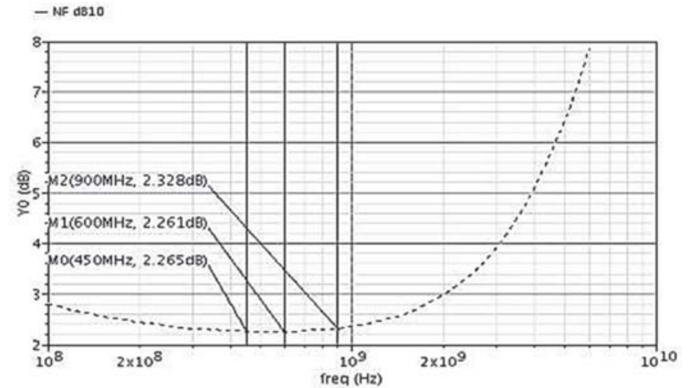

Figure 6. NF simulations for the prototype at 1.2 V.

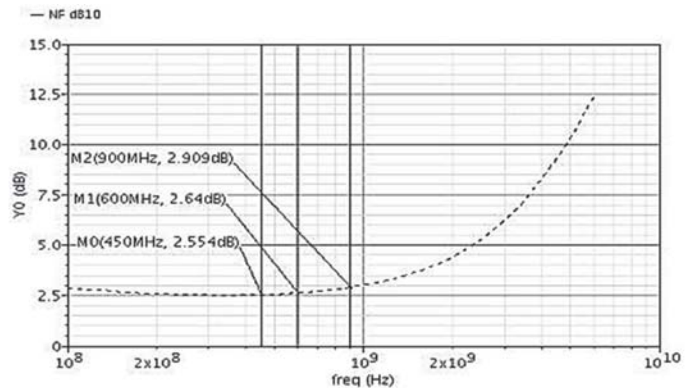

Figure 7. NF simulations for the prototype at 0.6 V.

A similar conclusion from Figs. 8 and 9, can be made with respect to the slightly lower gain that the LNA achieves when operating at 0.6 V.

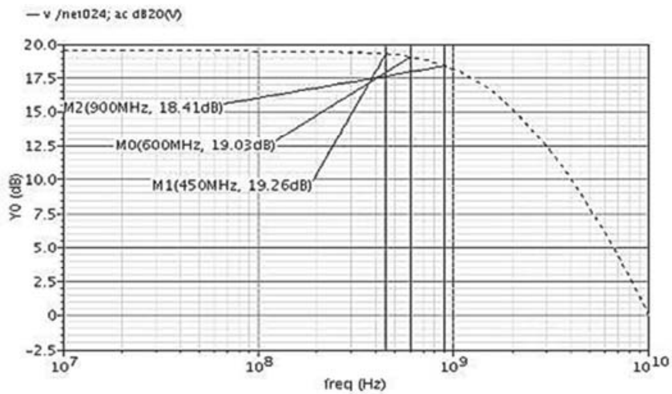

Figure 8. Gain simulation for the prototype with 1.2 V.

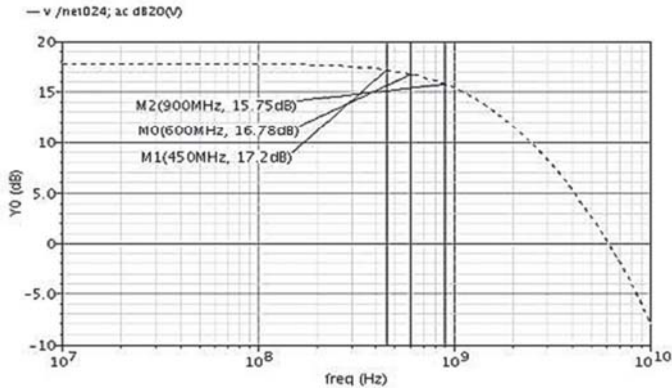

Figure 9. Gain simulation for the prototype at 0.6 V.

It is shown through Fig. 10 and Fig. 11 that the value of parameter S_{11} does not change significantly, meaning that the M_1 is maintaining a reasonable matching around -10 dB.

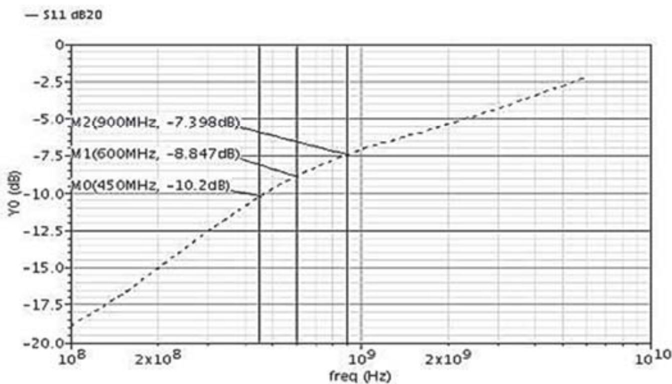

Figure 10. S_{11} parameter simulations for the prototype at 1.2 V.

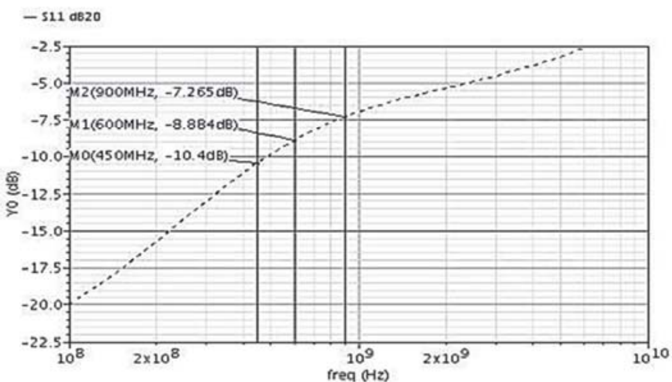

Figure 11. S_{11} parameter simulation for the prototype at 0.6 V.

It is also important to make a reference to simulations that show the performance improvements when using DTMOS configuration on certain transistors. The result shown in Fig. 12 demonstrates that by using DTMOS, an improvement of more than 1.5 dB for the gain and 0.2 dB for NF is possible.

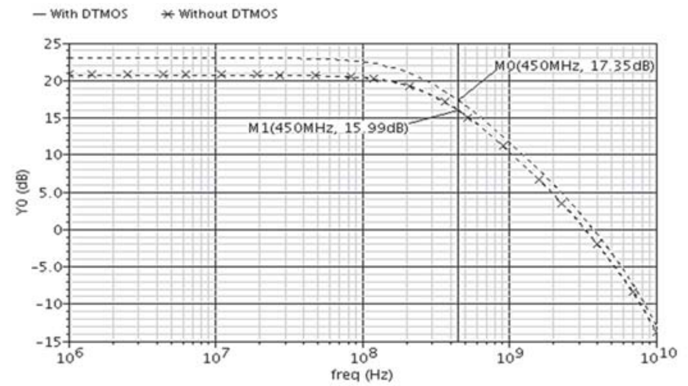

Figure 12. Comparison with and without DTMOS at 0.6 V.

Several PVT simulations were done considering 3 distinct temperatures cases. The obtained results are shown in Figs. 13, 14 and 15.

It is possible to note that, this circuit in general is capable to work in a range of temperatures between 0 and 85º for the three process cases.

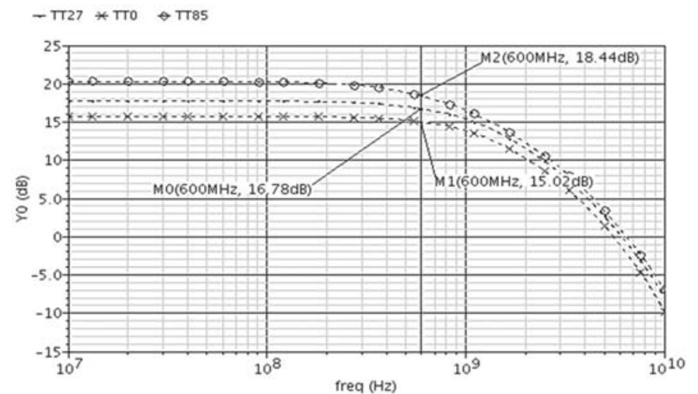

Figure 13. PVT simulation: TT case for the transistors.

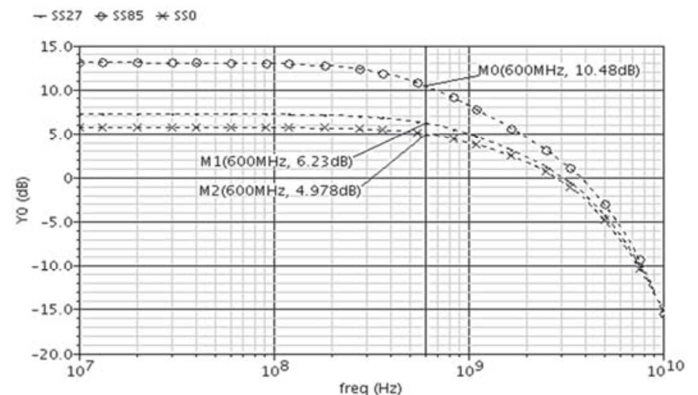

Figure 14. PVT simulation: SS case for the transistors.

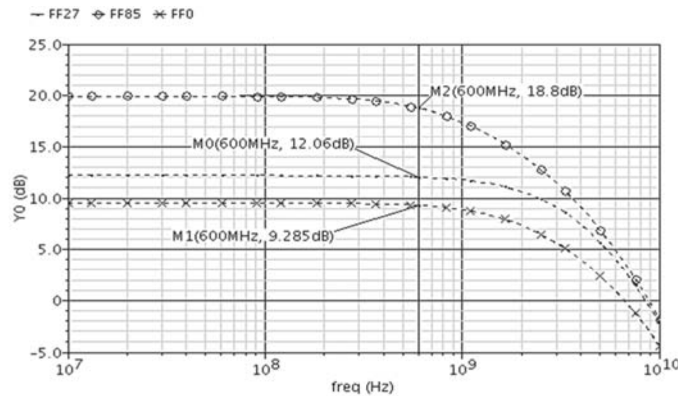

Figure 15. PVT simulation: FF case for the transistors.

Finally, in Table II a comparison with other designs is made.

TABLE II
COMPARISON WITH OTHER LNAS DESIGNS

	Tech (nm)	Band (GHz)	Av (dB)	NF (dB)	PDC (mW)	FOM (mW^{-1})
This work at 1.2 V	130	0.4-0.9	19.3	<2.3	11.8	1.15
This work at 0.6 V	130	0.4-0.9	17.2	<2.6	4	2.14
[10]*	180	0.1-0.9	15	<4.2	10	0.3
[11]*	180	0.5-0.9	16	<4.3	22	0.2

*Values obtained experimentally

V. CONCLUSION

In this paper we present a low power and low voltage LNA capable to work between 0.6 and 1.2 V with high gain and low NF, in 130 nm CMOS technology. Simulation results show that the gain of the LNA, operating at 1.2 V is enhanced to 19.3 dB and at 0.6 V is enhanced to 17.2 dB and the NF is below 2.3 dB for a power consumption of 4 mW operating at 0.6 V. The proposed circuit targets low power and low voltage operation in biomedical applications (ISM and WMTS).

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