The Architecture of a Low Phase Noise Low Power Delta-Sigma Fractional-N Synthesizer

Krzysztof Siwiec and Witold A. Pleskacz

***Abstract*—In this paper a new Delta-Sigma Fractional-N synthesizer architecture is presented. The synthesizer achieves low fractional spurs and quantization noise, which relaxes the trade-off between PLL bandwidth and phase noise. The proposed architecture is based on two delay lines, which are used to compensate the phase error resulting from fractional synthesis. Additionally, dedicated control and calibration circuitry is described. The synthesizer has been implemented in standard 130 nm CMOS technology, occupies 0.184 mm^2 silicon area and dissipates 3.6 mW of power from 1.2 V supply. Measurements show that the presented architecture achieves 30 dB phase noise reduction in comparison with a standard Delta-Sigma Fractional-N synthesizer. The integrated rms jitter is 2.76 ps and worst case fractional spur is -52 dBc.**

***Index Terms*—phase locked loop, PLL, Fractional-N, frequency synthesis, delay line, calibration**

I. Introduction

FRACTIONAL-N synthesizers are widely used in wireless communication integrated transceivers. Typically they are used as local oscillators. In the case when frequency or phase modulation is used in a communication system, Fractional-N PLLs are used as modulators. In such a case a new trade-off emerges between the phase noise and synthesizer bandwidth. Quantization noise cancelation realized by DAC-PFD (Digital-to-Analog Converter Phase-Frequency Detector) [1], [2] is the most commonly used solution to relax this trade-off. It makes it possible to achieve very low phase noise, but at the cost of high power consumption and large active circuit area. Those disadvantages are mainly caused by the DAC current noise and nonlinearity that force the designer to use mismatch shaping techniques.

In the proposed architecture delay lines are used to cancel phase error at the input of PFD instead of using DAC. A similar solution was presented in [3], where the Authors used one delay line to compensate the phase error. In this case the cancellation is limited to the delay of a single delay element, which is dependent on the manufacturing technology. What is more, if realizing a very fast delay element was possible, it would require a very long delay line to cover the range of phase error values possible in a Fractional-N synthesizer. Proposed solution overcomes this issue by using two delay lines, which allows to achieve multiple times (8-12) better resolution by just doubling the number of delay elements used.

K. Siwiec and W. Pleskacz are with the Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Poland

During recent years extensive work on the development of the so-called All Digital PLL (ADPLL) has been done [4]-[6]. ADPLLs use Time to Digital Converter (TDC) to convert phase error and process it in the digital domain. Most TDCs are based on a single delay line. Different techniques are used to improve the performance of ADPLLs, such as Phase Interpolation [6].

The proposed solution, which is based on two delay lines, can be used in both Charge Pump PLLs (CP-PLL) and ADPLLs. In this work the main focus is put on Charge Pump PLL. The described solution can easily be used to improve the phase noise performance of existing PLLs by simply adding a few blocks. The PLL architecture reduces the Sigma-Delta modulator phase noise impact on the synthesizer performance by 30 dB. The performance improvement is achieved by using two delay lines in the proposed architecture. The unit delay in each line is different and this difference is used to cancel the input phase error. By choosing the appropriate value of unit delay in each line it is possible to cover the whole range of phase errors using a small number of delay elements in each line. Because of PVT variations the unit delay value needs to be calibrated for both lines. The main features of the proposed solution are high phase-noise cancellation (30 dB), low power consumption and relatively small active area. The main drawback is higher low frequency phase noise level caused by the accumulated jitter, delay line mismatch and calibration error.

This paper is organized as follows. The proposed Fractional-N synthesizer architecture and the principle of its operation are presented in Section II. The phase noise analysis and model are introduced in Section III. Implementation details are shown in Section IV. Measurement results are discussed in Section V and conclusion is presented in Section VI.

II. Synthesizer Architecture

The architecture of the proposed synthesizer [7] is presented in Fig. 1. It consists of standard PLL building blocks, which are: phase-frequency detector (PFD) with charge pump (CP), loop filter, voltage controlled oscillator (VCO) and feedback divider. Additionally it consists of blocks that were added to the standard Fractional-N synthesizer (indicated by the shaded pattern). These blocks are: two delay lines with K unit delay elements, control block and calibration block. The delay lines

are used to cancel the phase error at the input of the PFD. The calibration block ensures that the unit delay in each delay line has the appropriate value. Fig. 2 presents the schematic of the control block, which is responsible for the operation of the synthesizer. It controls the feedback divider (N signal) and chooses which delay lines outputs should be connected to the PFD (Fb_{ctrl} – select output of feedback delay line, Ref_{ctrl} – select output of reference delay line).

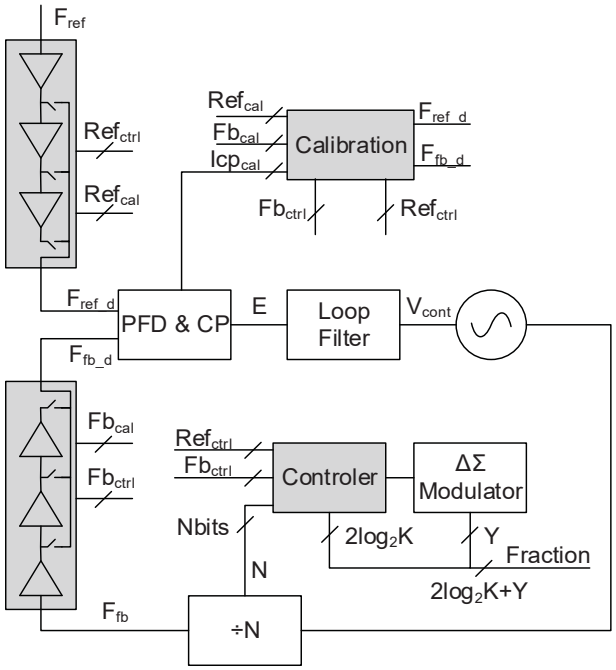

Fig. 1. Block diagram of the proposed Fractional-N synthesizer [7].

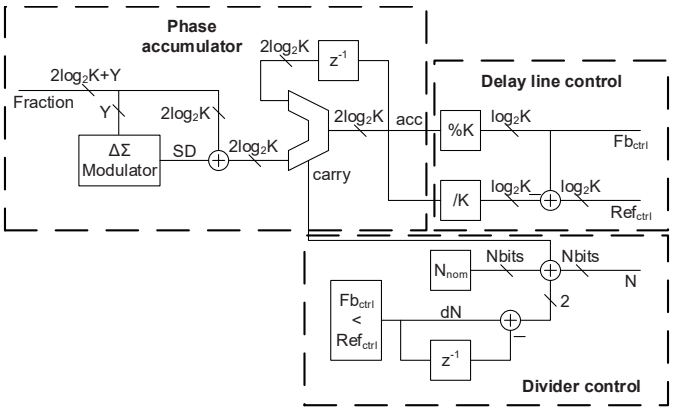

Fig. 2. High level schematic of the control block.

The principle of operation is to compensate the phase/time error at the input of the input of PFD. Let's consider a situation when the output frequency is:

$$f_{out} = f_{ref} \cdot (N_{nom} + \frac{Fraction}{K^2 2^Y}), \quad (1)$$

where N_{nom} and *Fraction* are integer and fractional part of PLL multiplication factor respectively, K is number of delay elements in each delay line and Y is bit resolution of Delta-Sigma modulator. The *Fraction* bit length is $2log_2K + Y$. In such a case the PFD input time difference would be given by equation:

$$\Delta t_{PFD\_ideal}[n] = n\frac{N_{nom}}{f_{ref}\cdot(N_{nom}+\frac{Fraction}{K^2 2^Y})} - \frac{n}{f_{ref}} = -\frac{n}{f_{out}}\frac{Fraction}{K^2 2^Y}. \quad (2)$$

Eq. (2) shows that the main goal is to generate linearly rising time error at the input of the PFD. In proposed architecture it is released by proper control of the delay lines output multiplexer and the divider. To make it possible it is assumed that the delay introduced be the delay lines is given by:

$$\Delta t_{ref} = Ref_{ctrl}[n]\frac{K}{K^2 f_{out}}, \quad (3)$$

$$\Delta t_{fb} = Fb_{ctrl}[n]\frac{K+1}{K^2 f_{out}}. \quad (4)$$

Under this assumption it can be proven [8] that using the control block as shown in fig. 2, allows to generate additional time difference at the PFD input equal to:

$$\Delta t_{PFD\_gen}[n] = \frac{n}{f_{out}}\frac{Fraction}{K^2 2^Y} + \frac{\sum_{i=1}^{n}(SD[n]-E[SD[n]])}{K^2}, \quad (5)$$

where *SD[n]* and *E[SD[n]]* is Delta-Sigma modulator output and its expected value. Combining Eq. (2) and (5) together gives final PFD input time error:

$$\Delta t_{PFD}[n] = \frac{\sum_{i=1}^{n}(SD[n]-E[SD[n]])}{K^2}.$$

As it can be seen only Delta-Sigma modulator error is still present, however it is suppressed by K^2 factor. This proves that presented architecture allows to achieve fractional multiplication factors, while significantly reducing the Delta-Sigma noise.

Additional advantage is that proposed solution can be easily implemented to existing Integer-N synthesizers as it does not require to change any important building block of CP-PLL.

Another interesting feature is that, if the values of unit delays were equal to those defined by (3) and (4), and no Delta-Sigma modulation was used, the synthesizer would not introduce any fractional spur or quantization noise. Of course it is not achievable in a real implementation. To keep unit delay values as close to (3) and (4) as possible, a calibration circuit was used. The main idea behind the calibration process is that the correlation between the delay line control signal and phase error at the input of PFD carries the information about unit delay error. Two correlators (one for each delay line) are used for calibration. Moreover, simulations showed that only the sign of the phase error is sufficient to achieve good calibration results. Additionally presented calibration procedure can be performed during normal PLL operation. The block diagram of the calibration circuit has been presented in Fig. 3.

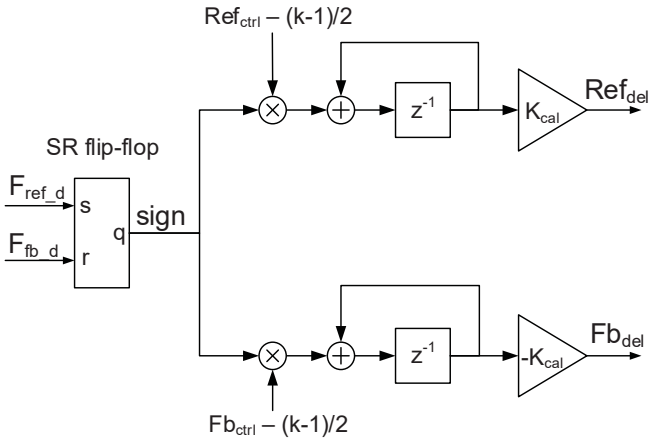

Fig. 3. Block diagram of the calibration circuit.

III. Phase Noise Analysis

As it was mentioned in Sec. II in the case when unit delay values of delay elements would be equal to the value given by (3) and (4) and no Delta-Sigma modulator is used, there would be no additional phase noise introduced in the circuit when compared to a standard Integer-N synthesizer. However, in reality the unit delay values are not exactly equal to (3), (4) and a Delta-Sigma modulator is used to increase the frequency resolution of the synthesizer. Those two factors introduce a phase error at the input of the PLL, which is illustrated in Fig. 4, where $e_Q[n]$ is the Delta-Sigma quantization noise, $\Delta t_Q[n]$ is the time domain noise resulting from the Delta-Sigma quantization noise, $\Delta t_D[n]$ is the time domain noise introduced by the non-ideality of the unit delay in delay lines, $\Delta\theta[n]$ is the phase noise at the input of synthesizer, $\Delta t_{ref\_e}(Ref_{ctrl})$ and $\Delta t_{fb\_e}(Fb_{ctrl})$ are delay errors in both delay lines. The delay errors for each line are given by the following equations:

$$\Delta t_{ref\_e}(Ref_{ctrl}) = Ref_{ctrl}\Delta t_{ref\_a} + \sum_{i=1}^{Ref_{ctrl}} \Delta t_{ref\_m}(i), \quad (6)$$

$$\Delta t_{fb\_e}(Fb_{ctrl}) = Fb_{ctrl}\Delta t_{fb\_a} + \sum_{i=1}^{Fb_{ctrl}} \Delta t_{fb\_m}(i), \quad (7)$$

where Δt_{ref_a} and Δt_{fb_a} are delay errors common for all unit delay elements, Δt_{ref_m} and Δt_{fb_m} represent delay mismatch with mean value equal to zero.

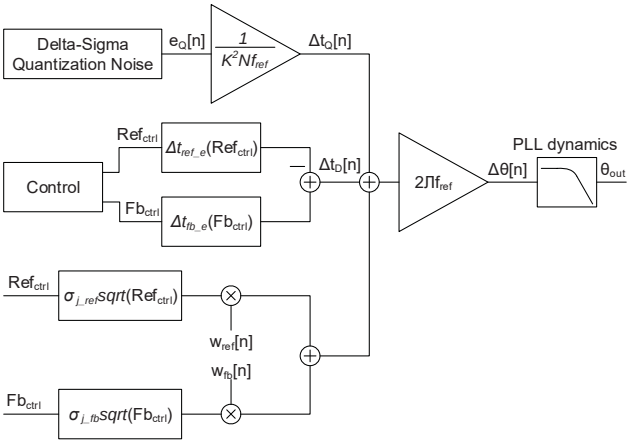

Fig. 4. Noise model of the proposed synthesizer.

There is one more noise source that is modeled and presented in Fig. 4. It is the accumulated jitter of the delay lines. The accumulated jitter for each line is modeled as:

$$j_{fb}[n] = \sigma_{jt\_fb}\sqrt{FB_{ctrl}[n]}w_{fb}[n], \quad (8)$$

$$j_{ref}[n] = \sigma_{jt\_ref}\sqrt{REF_{ctrl}[n]}w_{ref}[n], \quad (9)$$

where σ_{jt_fb} and σ_{jt_ref} is the jitter of the unit delay element in feedback and reference delay line respectively, $FB_{ctrl}[n]$ and $REF_{ctrl}[n]$ is the delay line control word for feedback and reference delay line respectively and $w_{fb}[n]$ and $w_{ref}[n]$ is the Gaussian distributed white noise with sigma equal to one.

To predict the phase noise performance of the PLL it is necessary to combine all the above noise sources with those present in a standard implementation of CP-PLL. The standard linear model can be used to predict the phase noise.

Based on the presented model, mathematical analysis and time-domain simulations, equations for the total phase noise (expressed as jitter) have been derived [8]. The output jitter can be expressed as a function of delay element calibration step [8]:

$$jt = \sqrt{\frac{K^2-1}{12}}\Delta t_{step}, \quad (10)$$

where Δt_{step} is the minimum trimming step of the delay element in a delay line and K is the number of delay elements in the delay line. The total output jitter may be related to a single delay element jitter in the following way [8]:

$$jt \approx \sqrt{1{,}9(K-1)\frac{f_c}{f_{ref}}}jt_{st}, \quad (11)$$

for a second order loop filter or [8]:

$$jt \approx \sqrt{2{,}2(K-1)\frac{f_c}{f_{ref}}}jt_{st}, \quad (12)$$

for a third order loop filter. The symbols f_c and f_{ref} stand for loop bandwidth and reference frequency, respectively and jt_{st} stands for the single delay element jitter.

Eq. (10) and (11) have been verified against time domain model implemented in Verilog-A of the proposed synthesizer. Fig. 5 and fig. 6 presents the comparison of obtained results. As it can be seen Eq. (10) gives the upper bound of jitter that can be expected, as it does not account for noise filtering inside the PLL. Results obtained for Eq. (11) are well matched with the simulation results. Verification of both equations shows their usefulness in the design process.

IV. Implementaion Details

The block diagram of the proposed Fractional-N PLL was already presented in Fig. 1. It has been implemented in standard 130 nm CMOS technology. The output frequency is around 1.5 GHz and one of the important design goals was to make the

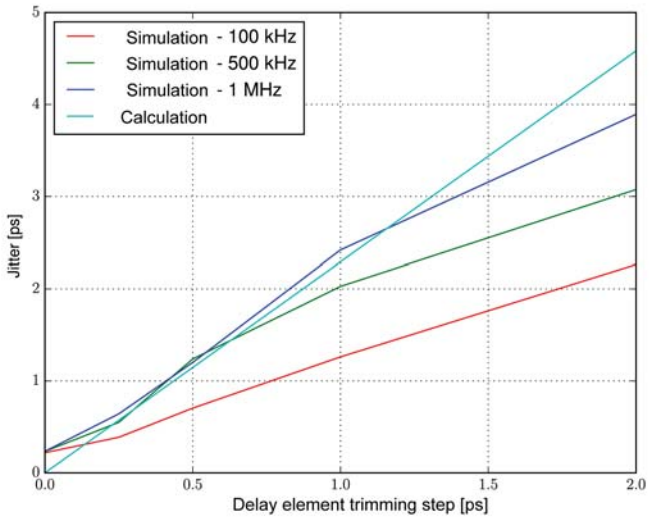

Fig. 5. Comparison of simulated and calculated PLL output jitter resulted from minimum trimming step of the delay element.

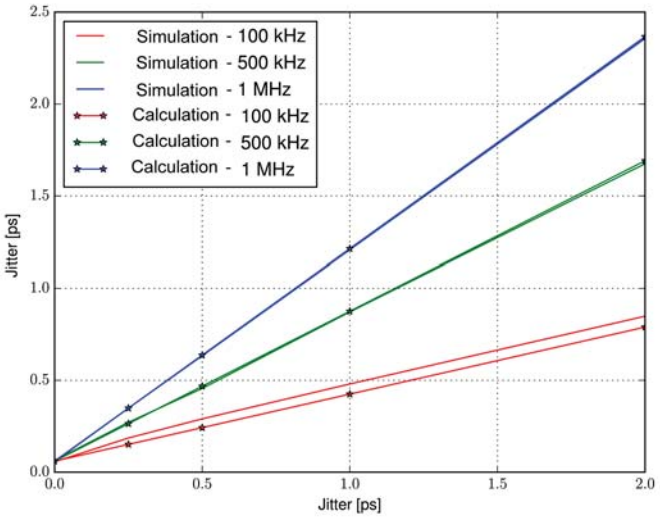

Fig. 6. Comparison of simulated and calculated PLL output jitter resulted from delay line element jitter.

circuit robust against PVT variations. The circuit works in all process corners, at temperatures between -40°C and 125ºC and with supply voltage from 1.08 V to 1.32 V. A current reusing [9] LC VCO with divider-by-2 has been used to generate the quadrature output signals. The VCO has a 2-bit frequency control, 4-bit amplitude control and a dedicated auto-calibration circuit to work properly in the whole range of PVT variations. A charge pump with current matching techniques [10] has been used to reduce the reference spurs. The bandwidth of the PLL was set to around 150 kHz.

Each of the two delay lines consists of 12 delay elements (current starved pseudo-differential delay elements – Fig. 7). The first two elements are used as dummies. This is necessary as the delay of a few first elements is different from the delay of further elements because of different rising and falling times of the input signals. Two elements are enough to stabilize the rising and falling times. The differences between the delays introduced by further elements are kept below a few percent. The last two elements are used to generate the clocking signals for digital control logic. The use of current-starved pseudo-differential delay elements makes it possible to achieve low power consumption and good matching. The disadvantage of using current starved inverters as delay elements is nonlinear tuning characteristics but tuning linearity is not necessary in the proposed architecture. Only monotonic behavior is required. The bias generation is common for all delay elements in each delay line. It provides 7-bit trimming, which makes it possible to achieve the necessary delay value over the whole PVT range.

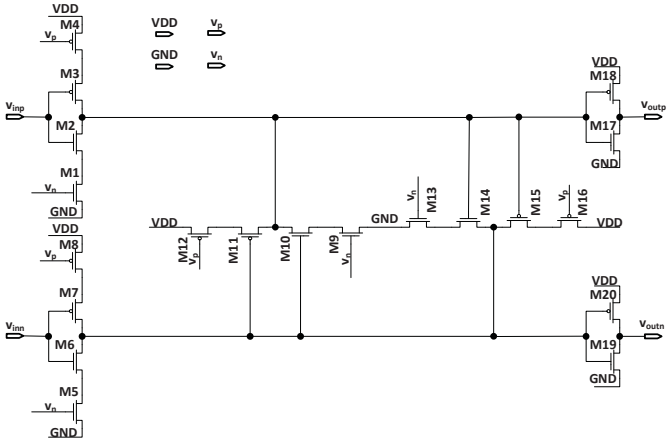

Fig. 7. Current starved pseudo-differential delay element schematic.

V. Measuremetns Results

The proposed PLL was designed and fabricated in the standard 130 nm CMOS technology. The die microphotograph and the layout have been presented in Fig. 8. The layout dimensions are 352 µm x 522 µm, which gives silicon area of 0.184 µm^2 [16]. The chip consumes 3.6 mW of power from 1.2 V supply voltage.

The measured phase noise (Fig. 9) at 100 kHz is -87 dBc and results mostly from the Charge Pump current noise. It could be reduced, though, by increasing the CP current. The integrated root mean square (rms) jitter, measured over the frequency offset range from 10 kHz to 50 MHz, is 2.76 ps. When the PLL is working as an Integer-N synthesizer, the rms integrated jitter is 2.38 ps. Because the phase noise from the Fractional-N part of the synthesizer is independent from the Integer-N part (which was verified by behavioral model simulations), the jitter introduced by the Fractional-N part is equal to $\sqrt{2.76^2 - 2.38^2} ps = 1.4\ ps$. The Fractional-N noise is mainly located in fractional spurs and results from the mismatch between delay elements. The worst case fractional spur (Fig. 10) is -52 dBc. This could be further reduced by employing the LMS spur reduction technique [11].

The measurement results were compared with the results obtained for the synthesizer working in the standard Sigma-Delta modulation mode (without delay lines). The maximum phase noise suppression is 30 dB (Fig. 11). It can be additionally noticed that for the Sigma-Delta Fractional-N synthesizer the in-band noise is also larger. This results from the fact that in presented design, the in-band noise is dominated

by the charge-pump noise. In the classic Fractional-N architecture, modulation of the division ratio of the feedback divider results in big, up to few periods of output signal, time error at the PFD input. This results in longer periods of time, when the up/down current source in charge pump are on, which finally results in much higher noise introduced by the charge pump. The measurements were performed using an Agilent EXA N9010A signal analyzer.

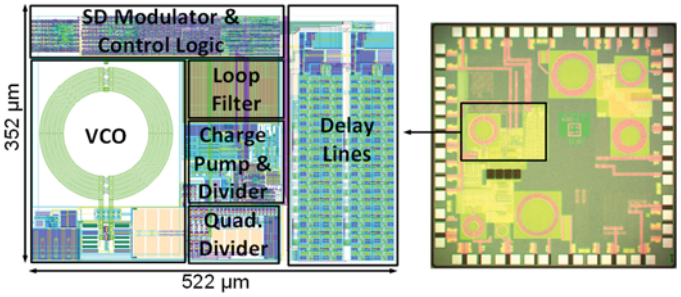

Fig. 8. Die photograph and layout of the proposed Fractional-N PLL.

Fig. 9. Measured Fractional-N PLL phase noise.

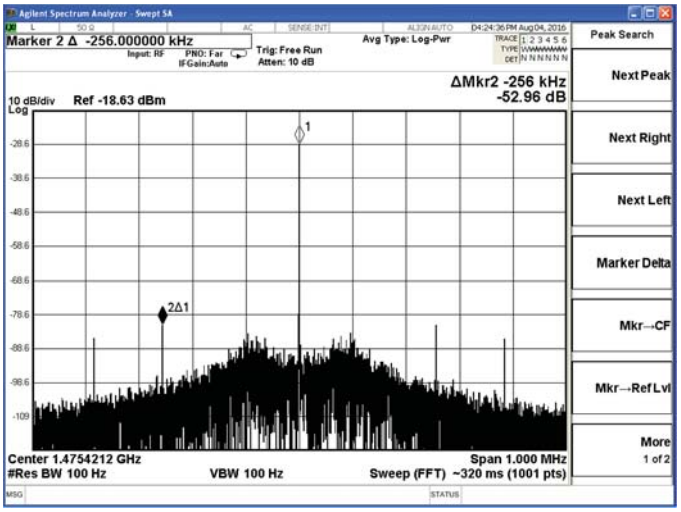

Fig. 10. Measured spectrum of the Fractional-N PLL

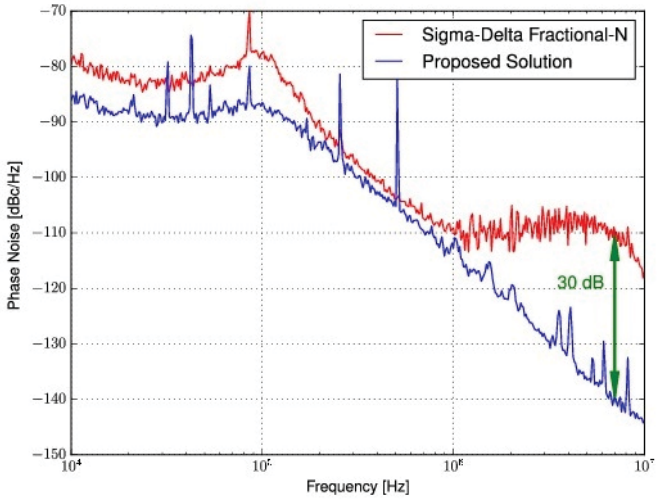

Fig. 11. Phase noise comparison between proposed and classic fractional-N synthesizer

The comparison of this work with other Fractional-N synthesizers aiming at Sigma-Delta noise reduction (see Table I) shows good performance in terms of Fractional spurs, noise suppression, power and area.

TABLE I.
PERFORMANCE SUMMARY AND COMPARISON

	[12]	[13]	[14]	[15]	This work
Technology [nm]	180 nm	180 nm	90 nm	65 nm	130 nm
Output [GHz]	6.12	3.24	5.4-6.5	3.5	1.45-1.65
Phase noise @ 100 kHz [dBc/Hz]	-102	-100	-95	-70	-85
Fractional spur [dBc]	-61	-50	N/A	-43	-53
Noise suppression [dB]	28	25	15	N/A	30
Power [mW]	26.1	43.2	28.8	21	3.6
Area [mm^2]	3.24	0.37	0.18	0.56	0.184

VI. CONLUSION

In this the paper new Fractional-N synthesizer architecture has been presented. The synthesizer has been implemented and prototyped in 130 nm CMOS technology Manufactured chips have been measured with positive results.

Measurement results showed high (30 dB) fractional noise suppression level and good phase noise performance. The integrated jitter is 2.76 ps and fractional spur level is -53 dB. Achieved power consumption is 3.6 mW. Above results show that the proposed new architecture allows to achieve both low phase noise level and low power consumption.

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Krzysztof Siwiec received the M.Sc. degree and the Ph.D. (with honors) in electronic engineering from the Warsaw University of Technology, Poland, in 2010 and 2016 respectively.

His doctoral research was related to frequency synthesis for low power wireless communication.

Since 2010 he has been with the Institute of Microelectronics and Optoelectronics (VLSI Engineering and Design Automation Division), at the same university, where he has been working on research and development of analog, RF and Mixed Signal integrated circuits for wireless communication and biomedical signal measurement. He has authored or coauthored over 20 works including: book chapters, papers published in conference proceedings and journals, and a patent application.

Dr. Krzysztof Siwiec has received various awards including: Diploma from Ministry of Science and Higher Education for research and development project in 2016 and Award for organizational achievements from Rector of Warsaw University of Technology in 2015. He is also a winner of international design contest organized by Europractice and United Microelectronic Corporation, awarded with free prototyping in UMC CMOS 130 nm technology.

Witold A. Pleskacz was born in Warsaw, Poland. He received the M.Sc. degree, the Ph.D. degree (with honors) and D.Sc. degree in electronic engineering from the Warsaw University of Technology, Poland, in 1983, 1995 and 2011 respectively.

Since 1984, he has been with the Institute of Microelectronics and Optoelectronics (VLSI Engineering and Design Automation Division), at the same university. He is an Associate Professor and Head of Warsaw ASIC Design Education Center (ADEC).

He spent one and half years as a Post Doctoral Researcher of Electrical and Computer Engineering at Carnegie Mellon University, Pittsburgh, PA (USA). He has authored or coauthored 6 books and over 100 papers published in conference proceedings and journals. His research interests include: methods of designing integrated circuits in submicron and nanometer CMOS technologies, computer-aided design methods and algorithms, layout-oriented manufacturing yield modeling, defect-based approaches to fault modeling, and design for manufacturability of ICs, defect oriented testing methodologies. He gave 20 invited talks and seminars in USA, Russia and 9 European countries. He has been a member of 9 international conference program committees: IEEE DFT, IEEE DDECS, IEEE YOT, CADSM, MEMSTECH, ECS, DSD-SS, ADEPT, MIXDES.

Prof. Pleskacz has received various awards including: Medal of National Education Commission in 2013, Ministry of National Education Award for teaching achievements in microelectronics in 1993, Ministry of Science and Higher Education Award for education achievements in microelectronics in 2006, 5 awards for scientific and teaching achievements from Rector of Warsaw University of Technology (in 1989, 1996, 2010, 2012 and 2013), and 3 *Golden Chalks* – Student Council of the Faculty Teaching Awards (in 2000, 2008 and 2012).