Design of a Novel Cascoded CMOS OpAmp with High Gain and ±1.5V Power Supply Voltage

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Abstract—The design of a novel CMOS operational amplifier with two differential input stages is described. Prototype circuits have been fabricated and measured successfully. By using a nested Miller compensation the stability of the operational amplifier is ensured. The layout has been created automatically by using the ALADIN tool [6-9]. The small signal model for the amplifier is depicted and the test results are presented.

Index Terms—Low-voltage, CMOS operational amplifier; Cascoded Stage; Nested Miller Compensation

I. INTRODUCTION

Basic issues of designing MOS amplifiers have accomplished significant progress in the last decades and many concepts have been presented.

An overview of operational amplifiers is given in [2-4]. Besides the single staged operational amplifiers, one of the most commonly used operational amplifier configuration is a CMOS two stage amplifier. The first stage is a differential stage with single-ended output, which suppresses the common mode voltage and amplifies the differential voltage. The second stage is an inverting output stage. In order to enhance the amplifier performance it will become necessary to improve the power-supply rejection, gain-bandwidth product and the stability.

In this paper a fully stable two-stage operational amplifier is presented. In order to improve the gain an additional differential stage is used. Due to the addition of a cascode in the input stage the high-frequency power supply rejection ratio is improved, but the compensation of the amplifier gets more difficult [1].

In the next section the architecture of the amplifier and its AC small-signal model are described. In Section III, the layout solution is explained. In Section IV, the measurement results are discussed and finally the conclusion is drawn.

II. OPAMP DESIGN

The structure of the CMOS operational amplifier is depicted in Fig. 1. As can be seen the amplifier uses two p-channel differential stages for the input, implemented by the transistors $M_1$, $M_2$ and $M_3$, $M_4$ and a p-channel cascode stage, formed by transistors $M_5$ and $M_6$. In [1] it has been shown that one approach to enhance AC PSRR is to find a feasibility to decouple the compensation capacitor from the gate of the output driver. The addition of the cascode transistors $M_5$ and $M_6$ permits the connection of the compensation capacitor $C_1$ to the source a cascode transistor. In this way the power supply rejection ratio is improved appreciable. The second Miller capacity connects the output with the two high ohmic points $P_1$ and $P_2$. The output stage is performed by the n-channel transistor $M_9$ and the p-channel transistor $M_{10}$, which is part of the current mirror formed by transistors $M_{10}$-$M_{13}$. The active load of the differential input stages is modeled by the n-channel transistors $M_7$ and $M_8$.

The fundamental idea of the presented amplifier based on an operational amplifier, which has been presented in [1]. Due to the use of an additional input stage it is possible to increase the DC voltage gain of the amplifier. The problem of frequency compensation has been solved by using a nested Miller compensation [5]. By applying the principle of the nested Miller compensation capacitor $C_2$ connects the gate of the transistor $M_9$ with the output. The normally used compensation capacitor can be omitted due to the low input resistance of the cascode stage. One disadvantage of this circuit is a reduction in common-mode input range as a result of the fall of voltage across the cascodes.
A. AC Small-Signal Model

In order to design the operational amplifier it is very useful to work with an appropriate small-signal model. The model can be used to determine the open-loop frequency response. Several elements have been combined and some small elements have been omitted in order to obtain a manageable AC small-signal model. The resulting model is shown in Fig. 2.

In this section a brief description for the model is given and can be followed in the context of Fig. 2. The current sources of the values \( \pm V_{igm} / 2 \) result from the action of the input source-coupled pair \( M_1 \) and \( M_2 \), the current sources of values \( \pm V_{igm} / 2 \) follow from the input pair \( M_1 \) and \( M_4 \). The voltages \( V_1 \) and \( V_2 \) in the model are the voltages on the two sides of the cascode transistor \( M_6 \). In an analogous manner the voltages \( V_3 \) and \( V_4 \) represent the voltages on both sides of the cascode transistor \( M_9 \). The conductance \( g_{01} \) is the sum of the small-signal conductance of transistor \( M_1 \) and the transconductance \( g_m \) and the substrate transconductance \( g_{sb} \) due to fixed gate bias of the cascode device. The small-signal conductance of transistor \( M_2 \) and \( M_4 \) respectively is represented by conductance \( g_2 \). The driver of the output stage of the amplifier \( M_9 \) is represented by the current source of value \( V_{2 gm} \) in shunt with the conductance \( g_{02} \), which includes the small-signal conductance of transistors \( M_2 \) and \( M_8 \). The small-signal capacitances are included to model the frequency response effectively. The compensation capacitor \( C_1 \) is connected from the output to the source of \( M_9 \). The gate to drain capacitance of transistor \( M_8 \) is realized by \( C_0 \). The compensation capacitor \( C_2 \) and the gate to drain capacitance of transistor \( M_6 \) are included in \( C_{02} \). The capacitor \( C_0 \) represents the gate-drain capacitor of the cascode transistors. The gate-source capacitance and junction capacitance of the cascode device are contained in capacitor \( C_{03} \). The parasitic capacitance of transistor \( M_5 \) is represented by \( C_{05} \).

It can be shown that for such an arrangement, the open-loop gain of the operational amplifier is given by (2).

Analysis of the ac small-signal model, after considerable algebra, results in the following polynomial transfer function:

\[
\frac{V}{V_i}(s) = s^3 a_{10} + s^2 a_{12} + s^3 a_{14} + s^3 a_{16} + s^2 a_{18} + s a_{20} + a_{22}
\]

where

\[
a_{10} = (-g_{m} C_{02} C_{1} C_{22} + \frac{1}{2} g_{m} C_{02} C_{2} C_{12} + g_{m} C_{02} C_{03} C_{22} + g_{m} C_{01} C_{12})
\]

\[
a_{12} = (g_{m} C_{02} C_{1} C_{12} + g_{m} C_{02} C_{03} C_{12} + g_{m} C_{01} C_{22})
\]

\[
a_{14} = (g_{m} C_{02} C_{1} C_{22} + g_{m} C_{02} C_{03} C_{22} + g_{m} C_{01} C_{12})
\]

\[
a_{16} = (g_{m} C_{02} C_{1} C_{12} + g_{m} C_{02} C_{03} C_{12} + g_{m} C_{01} C_{22})
\]

\[
a_{18} = (g_{m} C_{02} C_{1} C_{22} + g_{m} C_{02} C_{03} C_{22} + g_{m} C_{01} C_{12})
\]

\[
a_{20} = (g_{m} C_{02} C_{1} C_{12} + g_{m} C_{02} C_{03} C_{12} + g_{m} C_{01} C_{22})
\]

\[
a_{22} = (g_{m} C_{02} C_{1} C_{22} + g_{m} C_{02} C_{03} C_{22} + g_{m} C_{01} C_{12})
\]
\[ V_o = \frac{g_m \left( g_{m1} \left( g_{m2} + g_{m3} - g_{m3} \right) + g_{m2} \left( g_{m3} - g_{m3} \right) \right)}{g_{m4} + g_{m1} + g_{m4} + g_{o1} + g_{o2} + g_{o3} + \frac{g_{o1} \left( g_{o1} - g_{o3} \right)}{g_{o2} + g_{o3} + \frac{g_{o1} \left( g_{o1} - g_{o3} \right)}{g_{o2} + g_{o3} + \frac{g_{o1} \left( g_{o1} - g_{o3} \right)}}}} \]  

\[ \text{(2)} \]

### III. Layout

In Fig. 3 the layout of the presented cascoded amplifier is depicted. The operational amplifier has been fabricated with the IHP GmbH 0.25\( \mu \)m CMOS technology.

With the help of the layout generator environment of ALADIN [6-9] module generators have been written to create the layout of the presented cascoded operational amplifier automatically with minimum size. As can be seen a quite dense layout results. The current mirror, which has been formed by transistors M10-M13, is located in the upper half of the layout. Below of this module, the differential input stages M1, M2 and M3, M4 have been arranged on the left hand side. In the center of the layout the differential load (M7, M8), the n-channel output transistor M9 and the cascode stage, formed by transistors M5, M6 and M14, are positioned. The remaining space of the layout is taken by the capacitors C1 and C2.

### IV. Measurements

In this section, the measurement results are given. All measurements were performed with ±1.5 V power supply and a buffer amplifier with unity gain, 250 MHz bandwidth and an input capacitance of 2 pF. The measured performance data is given in Table I.

The open loop gain amounts 97 dB and the bandwidth of the amplifier is 14.3 MHz. The phase margin is 62°. A positive Slew Rate and a negative Slew Rate of 2.6 V/\( \mu \)s and 2.5 V/\( \mu \)s respectively were measured. The Common-Mode Rejection Ratio amounts 67 dB and an amplifier input offset voltage of 2.1 mV was determined. The low input offset is a result of a good process and a careful layout. The output swing of the cascoded amplifier amounts ±1.06 V. The measured positive Power Supply Rejection Ratio at 10 kHz is 67 dB. The negative Power Supply Rejection Ratio at 10 kHz is 65 dB.

In Fig. 4 the output time response of the operational amplifier for a rectangular input pulse is illustrated. The frequency response is depicted in Fig. 5 for \( I_{\text{Bias}} = 200 \mu \text{A} \) and a power supply of ±1.5 V.

Additional simulations have shown that the two compensation capacitors can be reduced. By using a passgate before capacitor C2, both capacitors C1 and C2 can be decreased to 40% of their original values. In this case the phase margin amounts 66°. In Fig. 6 the simulated gain response of the operational amplifier is shown. The gain of the whole amplifier is depicted by the topmost curve. The lowermost curve represents the gain by using the input differential stage M3, M4 only. The middle curve shows the gain of the amplifier using the input stage formed by transistors M1, M2 only. Further on the post-layout simulations reveal that it is possible to reduce the power supply voltage to ±1 V. In this case the simulated gain amounts 98 dB and the phase margin is 61.4°.

Despite the omission and aggregation of several small signal elements a large polynomial transfer function remains. Due to the complexity of equation (1), numerical methods have been applied to solve the given expression. Even though the denominator is a polynomial of 5th degree, the results of the numerical solution show that the following 3 poles are relevant only. The dominant pole is located a 93 Hz. The second and the third pole are at 7.9 MHz and 13.6 MHz. By solving the numerator of the transfer function three zeroes of importances are obtained. The first zero is located at 180 kHz. The additional two zeroes can be found at 9 MHz and 11.7 MHz.

<table>
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<tr>
<th>Parameter</th>
<th>Measured Results</th>
<th>Units</th>
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<tr>
<td>Supplies</td>
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<td>V</td>
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<tr>
<td>Open-Loop Gain</td>
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<td>dB</td>
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<tr>
<td>Phase Margin</td>
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<td>°</td>
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<td>Bandwidth</td>
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<td>Input Offset Voltage</td>
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<td>Output Swing</td>
<td>±1.06</td>
<td>V</td>
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<tr>
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<tr>
<td>1 kHz</td>
<td>80</td>
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<td>57</td>
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<td>1 kHz</td>
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<td>dB</td>
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<tr>
<td>100 kHz</td>
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<td>Negative Slew Rate</td>
<td>2.5</td>
<td>V/( \mu )s</td>
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<tr>
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<td>mm²</td>
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</table>
V. CONCLUSIONS

A cascoded operational amplifier with two differential input stages and a power supply voltage of ±1.5 V has been presented. The layout of the circuit has been created with the help of the ALADIN package [6-9]. By using the AC small-signal model it is possible to show that the presented amplifier has three poles and three zeroes. Obviously a pole and a zero are compensated at around 10 MHz.

Prototype circuits have been fabricated and measured in order to verify the amplifier’s stability. A voltage gain of 97 dB and a unity gain bandwidth larger than 14 MHz were measured for ±1.5 supply voltage. Due to the use of the nested Miller compensation the amplifier has a sufficient phase margin and therefore it is fully stable. The measurements show that the transient response is comparable to an amplifier, which shows one pole only. The cascoded operational amplifier offers an excellent high-frequency power supply rejection ratio.

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REFERENCES