Design of a Novel Cascoded CMOS OpAmp with High Gain and ±1.5V Power Supply Voltage

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***Abstract*—The design of a novel CMOS operational amplifier with two differential input stages is described. Prototype circuits have been fabricated and measured successfully. By using a nested Miller compensation the stability of the operational amplifier is ensured. The layout has been created automatically by using the ALADIN tool [6-9]. The small signal model for the amplifier is depicted and the test results are presented.**

***Index Terms*—Low-voltage, CMOS operational amplifier; Cascoded Stage; Nested Miller Compensation**

I. Introduction

Basic issues of designing MOS amplifiers have accomplished significant progress in the last decades and many concepts have been presented.

An overview of operational amplifiers is given in [2-4]. Besides the single staged operational amplifiers, one of the most commonly used operational amplifier configuration is a CMOS two stage amplifier. The first stage is a differential stage with single-ended output, which suppresses the common mode voltage and amplifies the differential voltage. The second stage is an inverting output stage. In order to enhance the amplifier performance it will become necessary to improve the power-supply rejection, gain-bandwidth product and the stability.

In this paper a fully stable two-stage operational amplifier is presented. In order to improve the gain an additional differential stage is used. Due to the addition of a cascode in the input stage the high-frequency power supply rejection ratio is improved, but the compensation of the amplifier gets more difficult [1].

In the next section the architecture of the amplifier and its AC small-signal model are described. In Section III, the layout solution is explained. In Section IV, the measurement results are discussed and finally the conclusion is drawn.

II. OpAmp Design

The structure of the CMOS operational amplifier is depicted in Fig. 1. As can be seen the amplifier uses two p-channel differential stages for the input, implemented by the

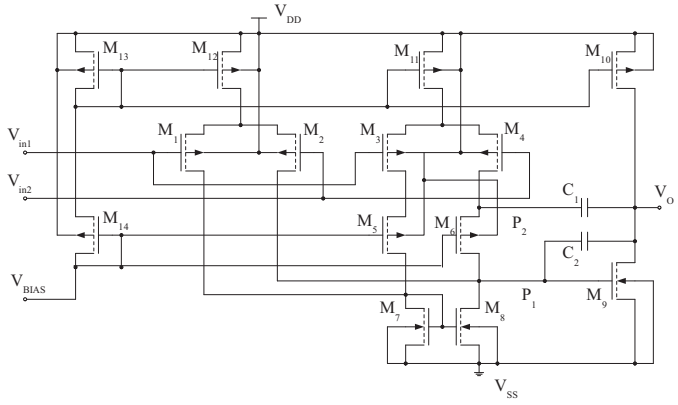

Figure 1. Schematic of the cascoded operational amplifier

transistors M_1, M_2 and M_3, M_4 and a p-channel cascode stage, formed by transistors M_5 and M_6. In [1] it has been shown that one approach to enhance AC PSRR is to find a feasibility to decouple the compensation capacitor from the gate of the output driver. The addition of the cascode transistors M_5 and M_6 permits the connection of the compensation capacitor C_1 to the source a cascode transistor. In this way the power supply rejection ratio is improved appreciable. The second Miller capacity connects the output with the two high ohmic points P_1 and P_2. The output stage is performed by the n-channel transistor M_9 and the p-channel transistor M_{10}, which is part of the current mirror formed by transistors M_{10}-M_{13}. The active load of the differential input stages is modeled by the n-channel transistors M_7 and M_8.

The fundamental idea of the presented amplifier based on an operational amplifier, which has been presented in [1]. Due to the use of an additional input stage it is possible to increase the DC voltage gain of the amplifier. The problem of frequency compensation has been solved by using a nested Miller compensation [5]. By applying the principle of the nested Miller compensation capacitor C_2 connects the gate of the transistor M_9 with the output. The normally used compensation capacitor can be omitted due to the low input resistance of the cascode stage. One disadvantage of this circuit is a reduction in common-mode input range as a result of the fall of voltage across the cascodes.

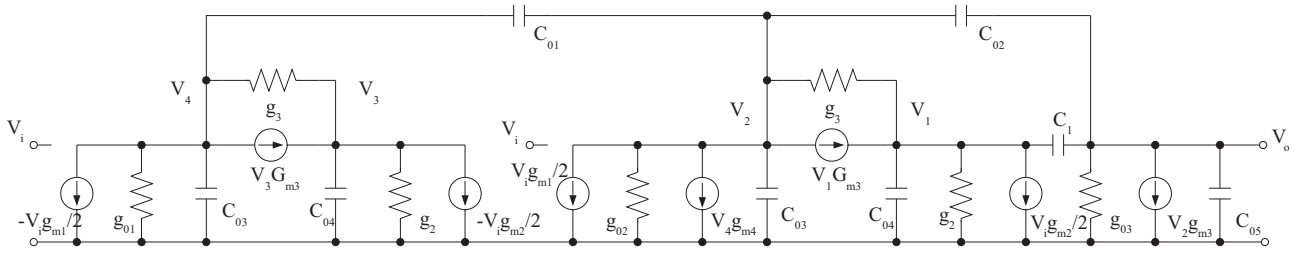

Figure 2. AC small-signal model for the cascoded operational amplifier of Figure 1

A. AC Small-Signal Model

In order to design the operational amplifier it is very useful to work with an appropriate small-signal model. The model can be used to determine the open-loop frequency response. Several elements have been combined and some small elements have been omitted in order to obtain a manageable AC small-signal model. The resulting model is shown in Fig.2.

In this section a brief description for the model is given and can be followed in the context of Fig. 2. The current sources of the values $\pm V_i g_{m1}/2$ result form the action of the input source-coupled pair M_1 and M_2, the current sources of values $\pm V_i g_{m2}/2$ follow from the input pair M_3 and M_4. The voltages V_1 and V_2 in the model are the voltages on the two sides of the cascode transistor M_6. In an analogous manner the voltages V_3 and V_4 represent the voltages on both sides of the cascode transistor M_5. The conductance g_{01} is the sum of the small-signal conductance of transistor M_1 and the transconductance of transistor M_7. The sum of the small-signal conductance of M_2 and M_8 is included in the conductance g_{02}. The dependent source V_1G_{m3} represents the transconductance of cascode device M_6, whereas g_3 models its associated drain to source conductance. The current is controlled by voltage V_1. In a uniform manner the current source V_3G_{m3} represents the transconductance of the cascode transistor M_5. In contrast to the cascode transistor M_6 the current is controlled by voltage V_3. The effective transconductance G_{m3} is the sum of the gate-source transconductance g_m and the substrate transconductance g_{mb}, due to fixed gate bias of the cascode device. The small-signal conductance of transistor M_2 and M_4 respectively is represented by conductance g_2. The driver of the output stage of the amplifier M_9 is represented by the current source of value V_2g_{m3} in shunt with the conductance g_{03}, which includes the small-signal conductance of transistors M_9 and M_{10}.

The small-signal capacitances are included to model the frequency response effectively. The compensation capacitor C_1 is connected from the output to the source of M_6. The gate to drain capacitance of transistor M_8 is realized by C_{01}. The compensation capacitor C_2 and the gate to drain capacitance of transistor M_9 are included in C_{02}. The capacitor C_{03} represents the gate-drain capacitor of the cascode transistors. The gate-source capacitance and junction capacitance of the cascode device are contained in capacitor C_{04}. The parasitic capacitance of transistor M_{10} is represented by C_{05}.

It can be shown that for such an arrangement, the open-loop gain of the operational amplifier is given by (2).

Analysis of the ac small-signal model, after considerable algebra, results in the following polynomial transfer function:

$$\frac{V_o}{V_i}(s)=\frac{s^4a_{01}+s^3a_{02}+s^2a_{03}+sa_{04}+a_{05}}{s^5a_{11}+s^4a_{12}+s^3a_{13}+s^2a_{14}+sa_{15}+a_{16}} \qquad (1)$$

where

$$a_{01}=(-g_{m2}C_{04}\delta_{25}C_1\delta_{22}+\tfrac{1}{2}g_{m1}C_{02}\delta_{24}C_{04}\delta_{25}),$$

$$a_{02}=-g_{m4}(g_{m2}C_1C_{01}+\tfrac{1}{2}C_{02}g_{m1}C_{04})\delta_{24}-\tfrac{1}{2}(g_{m1}g_{m3}\delta_{24}-g_{m1}C_{02}\delta_{11})C_{04}\delta_{25}$$
$$+(\delta_{11}\delta_{25}+C_{04}\delta_{13})(\tfrac{1}{2}g_{m1}C_{02}\delta_{24}-g_{m2}C_1\delta_{22})+C_{04}\delta_{25}(-g_{m2}\delta_{12}C_{02}-g_{m2}C_1\delta_{14}),$$

$$a_{03}=-\tfrac{1}{2}g_{m1}g_{m3}\delta_{11}C_{04}\delta_{25}+(\delta_{11}\delta_{25}+C_{04}\delta_{13})(-\tfrac{1}{2}(g_{m1}g_{m3}\delta_{24}-g_{m1}C_{02}\delta_{11})-(g_{m2}\delta_{12}C_{02}+g_{m2}C_1\delta_{14}))$$
$$+(\delta_{11}\delta_{13}-g_3\delta_{12})(\tfrac{1}{2}g_{m1}C_{02}\delta_{24}-g_{m2}C_1\delta_{22})-g_{m4}(-\tfrac{1}{2}g_{m3}g_{m1}C_{04}-C_{02}(g_{m2}\delta_{12}-\tfrac{1}{2}g_{m1}\delta_{11}))\delta_{24}$$
$$-g_{m4}(g_{m2}C_1C_{01}+\tfrac{1}{2}C_{02}g_{m1}C_{04})\delta_{11}+C_{04}\delta_{25}g_{m2}\delta_{12}g_{m3},$$

$$a_{04}=(\delta_{11}\delta_{25}+C_{04}\delta_{13})(-\tfrac{1}{2}g_{m1}g_{m3}\delta_{11}+g_{m2}\delta_{12}g_{m3})$$
$$-\tfrac{1}{2}(\delta_{11}\delta_{13}-g_3\delta_{12})((g_{m1}g_{m3}\delta_{24}-g_{m1}C_{02}\delta_{11})+(-g_{m2}\delta_{12}C_{02}-g_{m2}C_1\delta_{14}))$$
$$-g_{m4}g_{m3}(g_{m2}\delta_{12}-\tfrac{1}{2}g_{m1}\delta_{11})\delta_{24}-g_{m4}(-\tfrac{1}{2}g_{m3}g_{m1}C_{04}-C_{02}(g_{m2}\delta_{12}-\tfrac{1}{2}g_{m1}\delta_{11}))\delta_{11},$$

$$a_{05}=g_{m4}g_{m3}(g_{m2}\delta_{12}-\tfrac{1}{2}g_{m1}\delta_{11})\delta_{11}+(\delta_{11}\delta_{13}-g_3\delta_{12})(-\tfrac{1}{2}g_{m1}g_{m3}\delta_{11}+g_{m2}\delta_{12}g_{m3}),$$

$$a_{11}=C_{04}\delta_{25}(\delta_{22}(C_1^2-\delta_{23}\delta_{21})+C_{02}^2\delta_{24}),$$

$$a_{12}=-(C_{02}g_{m3}\delta_{24}-C_{02}^2\delta_{11})C_{04}\delta_{25}+(\delta_{11}\delta_{25}+C_{04}\delta_{13})(C_{02}^2\delta_{24}+\delta_{22}(C_1^2-\delta_{23}\delta_{21}))$$
$$+g_{m4}\delta_{24}C_{01}(C_1^2-\delta_{23}\delta_{21})+C_{04}\delta_{25}(\delta_{14}(C_1^2-\delta_{23}\delta_{21})+\delta_{22}(-g_{03}\delta_{21}-\delta_{23}\delta_{11})+\delta_{12}C_{02}C_1),$$

$$a_{13}=(\delta_{11}\delta_{13}-g_3\delta_{12})(\delta_{22}(C_1^2-\delta_{23}\delta_{21})+C_{02}^2\delta_{24})-C_{02}g_{m3}\delta_{11}C_{04}\delta_{25}$$
$$+(\delta_{11}\delta_{25}+C_{04}\delta_{13})((\delta_{14}(C_1^2-\delta_{23}{}^*\delta_{21})+\delta_{22}(-g_{03}\delta_{21}-\delta_{23}\delta_{11})+\delta_{12}C_{02}C_1)-(C_{02}g_{m3}\delta_{24}-C_{02}^2\delta_{11}))$$
$$+C_{04}\delta_{25}(\delta_{14}(-g_{03}\delta_{21}-\delta_{23}\delta_{11})-\delta_{22}g_{03}\delta_{11}-\delta_{12}(g_{m3}C_1-g_3\delta_{23}))$$
$$+g_{m4}\delta_{11}(C_1^2C_{01}-C_{01}\delta_{23}\delta_{21})+g_{m4}\delta_{24}(-C_{01}g_{03}\delta_{21}-C_{01}\delta_{23}\delta_{11})$$

$$a_{14}=(\delta_{11}\delta_{25}+C_{04}\delta_{13})(-C_{02}g_{m3}\delta_{11}+(\delta_{11}\delta_{14}g_{03}((-\delta_{21}-\delta_{23})-\delta_{22})-\delta_{12}(g_{m3}C_1-g_3\delta_{23})))$$
$$+(\delta_{11}\delta_{13}-g_3\delta_{12})(-(C_{02}g_{m3}\delta_{24}-C_{02}^2\delta_{11})+(\delta_{14}(C_1^2-\delta_{23}\delta_{21})+\delta_{22}(-g_{03}\delta_{21}-\delta_{23}\delta_{11})+\delta_{12}C_{02}C_1))$$
$$+g_{m4}g_{03}\delta_{11}((-C_{01}\delta_{21}-C_{01}\delta_{23}\delta_{11})-\delta_{24}C_{01})+g_{03}C_{04}\delta_{25}(-\delta_{14}\delta_{11}+\delta_{12}g_3),$$

$$a_{15}=\delta_{11}(\delta_{11}\delta_{13}-g_3\delta_{12})((\delta_{14}g_{03}((-g_{03}\delta_{21}-\delta_{23}\delta_{11})-(\delta_{22}-\delta_{12}(g_{m3}C_1-g_3\delta_{23})))-C_{02}g_{m3}))$$
$$+g_{03}(\delta_{11}\delta_{25}+C_{04}\delta_{13})(-\delta_{14}\delta_{11}+\delta_{12}g_3)-g_{m4}\delta_{11}^2C_{01}g_{03},$$

$$a_{16}=(\delta_{11}\delta_{13}-g_3\delta_{12})(-\delta_{14}g_{03}\delta_{11}+\delta_{12}g_3g_{03}),$$

$$\delta_{11}=g_2+g_3-G_{m3}$$
$$\delta_{12}=g_3-G_{m3}$$
$$\delta_{13}=g_{01}+g_3$$
$$\delta_{14}=g_{02}+g_3$$

and

$$\delta_{21}=C_1+C_{04}$$
$$\delta_{22}=C_{01}+C_{02}+C_{03}$$
$$\delta_{23}=C_{01}+C_{02}+C_{05}$$
$$\delta_{24}=C_1+C_{04}-g_3C_1$$
$$\delta_{25}=C_{01}+C_{03}.$$

$$\frac{V_o}{V_i} = \frac{g_{m3}\{g_{m1}(g_2+g_3-G_{m3})+g_{m2}(g_3-G_{m3})\}}{\frac{2g_{03}(g_2+g_3-G_{m3})}{g_{m4}+g_{01}+g_3+\frac{g_3(G_{m3}-g_3)}{g_2+g_3-G_{m3}}}\left(g_{01}+g_3+\frac{g_3(G_{m3}-g_3)}{g_2+g_3-G_{m3}}\right)\left(g_{02}+g_3+\frac{g_3(G_{m3}-g_3)}{g_2+g_3-G_{m3}}\right)} \quad (2)$$

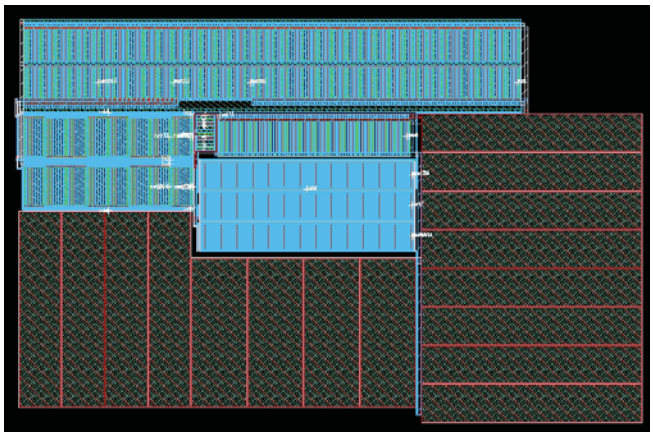

Figure 3. Layout of the cascoded operational amplifier

TABLE I. AMPLIFIER PERFORMANCE SUMMARY

Parameter	Measured Results	Units
Supplies	±1.5	V
Open-Loop Gain	97	dB
Phase Margin	62	°
Bandwidth	14.3	MHz
Input Offset Voltage	-2.1 m	mV
Output Swing	±1.06	V
CMRR	67	dB
PSRR+ at DC		
1 kHz	80	dB
10 kHz	67	dB
100 kHz	57	dB
PSRR- at DC		
1 kHz	76	dB
10 kHz	65	dB
100 kHz	56	dB
Positive Slew Rate	2.6	V/µs
Negative Slew Rate	2.5	V/µs
Die Area	0.17	mm²

Despite the omittance and aggregation of several small signal elements a large polynomial transfer function remains. Due to the complexity of equation (1), numerical methods have been applied to solve the given expression. Even though the denominator is a polynomial of 5th degree, the results of the numerical solution show that the following 3 poles are relevant only. The dominant pole is located a 93 Hz. The second and the third pole are at 7.9 MHz and 13.6 MHz. By solving the numerator of the transfer function three zeroes of importances are obtained. The first zero is located at 180 kHz. The additional two zeroes can be found at 9 MHz and 11.7 MHz.

III. LAYOUT

In Fig. 3 the layout of the presented cascoded amplifier is depicted. The operational amplifier has been fabricated with the IHP GmbH 0.25µm CMOS technology.

With the help of the layout generator environment of ALADIN [6-9] module generators have been written to create the layout of the presented cascoded operational amplifier automatically with minimum size. As can be seen a quite dense layout results. The current mirror, which has been formed by transistors M_{10}-M_{13}, is located in the upper half of the layout. Below of this module, the differential input stages M_1, M_2 and M_3, M_4 have been arranged on the left hand side. In the center of the layout the differential load (M_7, M_8), the n-channel output transistor M_9 and the cascode stage, formed by transistors M_5, M_6 and M_{14}, are positioned. The remaining space of the layout is taken by the capacitors C_1 and C_2.

IV. MEASUREMENTS

In this section, the measurement results are given. All measurements were performed with ±1.5 V power supply and a buffer amplifier with unity gain, 250 MHz bandwidth and an input capacitance of 2 pF. The measured performance data is given in Table I.

The open loop gain amounts 97 dB and the bandwidth of the amplifier is 14.3 MHz. The phase margin is 62°. A positive Slew Rate and a negative Slew Rate of 2.6 V/µs and 2.5 V/µs respectively were measured. The Common-Mode Rejection Ratio amounts 67 dB and an amplifier input offset voltage of 2.1 mV was determined. The low input offset is a result of a good process and a careful layout. The output swing of the cascoded amplifier amounts ±1.06 V. The measured positive Power Supply Rejection Ratio at 10 kHz is 67 dB. The negative Power Supply Rejection Ratio at 10 kHz is 65 dB.

In Fig. 4 the output time response of the operational amplifier for a rectangular input pulse is illustrated. The frequency response is depicted in Fig. 5 for I_{Bias} = 200 µA and a power supply of ±1.5 V.

Additional simulations have shown that the two compensation capacitors can be reduced. By using a passgate before capacitor C_2, both capacitors C_1 and C_2 can be decreased to 40% of their original values. In this case the phase margin amounts 66°. In Fig. 6 the simulated gain response of the operational amplifier is shown. The gain of the whole amplifier is depicted by the topmost curve. The lowermost curve represents the gain by using the input differential stage M_3, M_4 only. The middle curve shows the gain of the amplifier using the input stage formed by transistors M_1, M_2 only. Further on the post-layout simulations reveal that it is possible to reduce the power supply voltage to ±1 V. In this case the simulated gain amounts 98 dB and the phase margin is 61.4°.

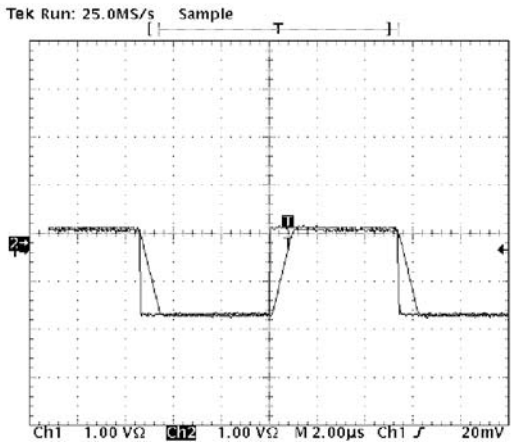

Figure 4. Output time response for a rectangular input pulse

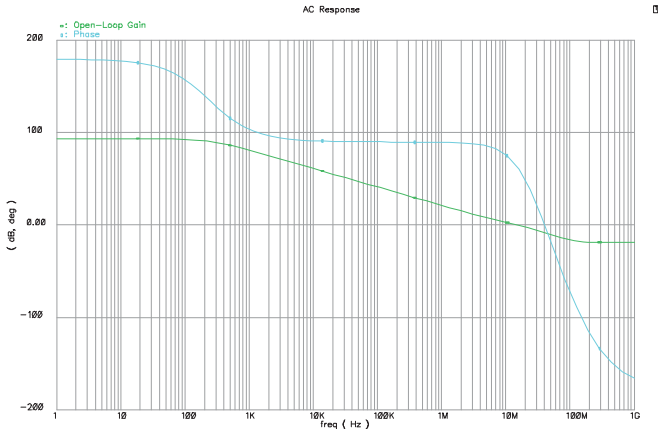

Figure 5. Bode plot of the cascoded operational amplifier

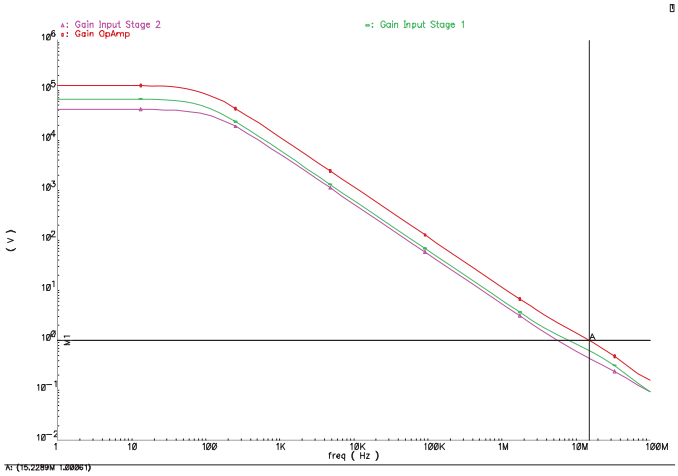

Figure 6. Gain response of the input stages and the whole amplifier

V. Conclusions

A cascoded operational amplifier with two differential input stages and a power supply voltage of ±1.5 V has been presented. The layout of the circuit has been created with the help of the ALADIN package [6-9]. By using the AC small-signal model it is possible to show that the presented amplifier has three poles and three zeroes. Obviously a pole and a zero are compensated at around 10 MHz.

Prototype circuits have been fabricated and measured in order to verify the amplifiers stability. A voltage gain of 97 dB and a unity gain bandwidth larger than 14 MHz were measured for ±1.5 supply voltage. Due to the use of the nested Miller compensation the amplifier has a sufficient phase margin and therefore it is fully stable. The measurements show that the transient response is comparable to an amplifier, which shows one pole only. The cascoded operational amplifier offers an excellent high-frequency power supply rejection ratio.

Acknowledgement

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References

[1] D.B. Ribner and M.A. Copeland, “Design Techniques for Cascoded CMOS Op Amps with Improved PSRR and Common-Mode Input Range,” IEEE J. Solid-State Circuits, vol. SC-19, pp. 919-925, December 1984.

[2] P.R. Gray and R.G. Meyer, “MOS operational amplifier design – A tutorial overview,” IEEE J. Solid-State Circuits, vol. SC-17, pp. 969-982, December 1982.

[3] K.R. Laker and W.M.C. Sansen, “Design of Analog Integrated Circuits and Systems,” McGraw-Hill, Inc. 1994.

[4] F. Roewer and U. Kleine, “A Novel Class of Complementary Folded-Cascoded Opamps for Low Voltage,” IEEE J. Solid-State Circuits, vol. 37, No. 8, pp. 1080-1083, August 2002.

[5] R.G.H. Eschauzier and J.H. Huijsing, ”Fequency Compensation Techniques for Low-Power Operational Amplifiers,” Kluwer Academic Publishers, 1995.

[6] M. Wolf, U. Kleine and B. Hosticka, “A Novel Module Generator Environment,” Proc. The European Design & Test Conference, pp. 388-392, March 1996.

[7] M. Wolf and U. Kleine, “Reliability Driven Module Generation for Analog Layouts,” ISCAS 99, vol. 6, pp. 412-415, June 1999.

[8] L. Zhang, U. Kleine and Y. Jiang, “An Automated Design Tool for Analog Layouts,” IEEE Trans. On VLSI, vol. 14, No. 8, pp. 881-894, August 2006.

[9] B. Lipka and U. Kleine, “Design of a Linear Power Amplifier with ±1.5V Power Supply Using ALADIN,” 17th International Workshop PATMOS 2007, pp. 97-106, September 2007.